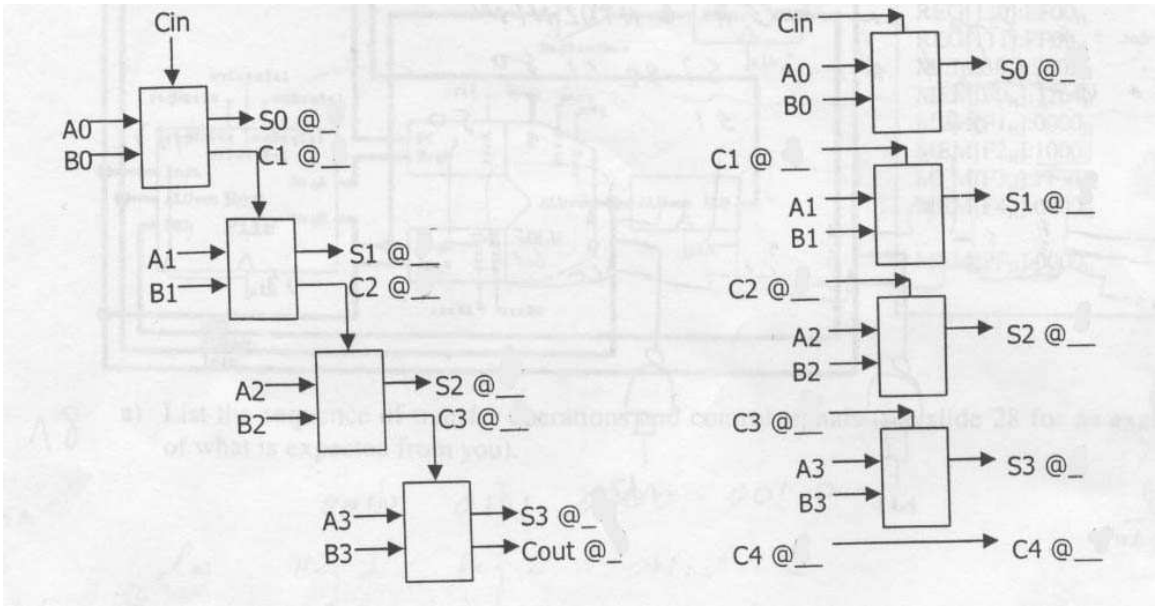
**EECS 150 Fall 2001 3rd Midterm**

**Professor: Vivek Subramanian**

## Problem 1

Recalculate the various propogation delays in a 4-bit carry lookahead adder and a ripple adder assuming that XOR gates have twice the delay of all other gates.



**Problem 2**

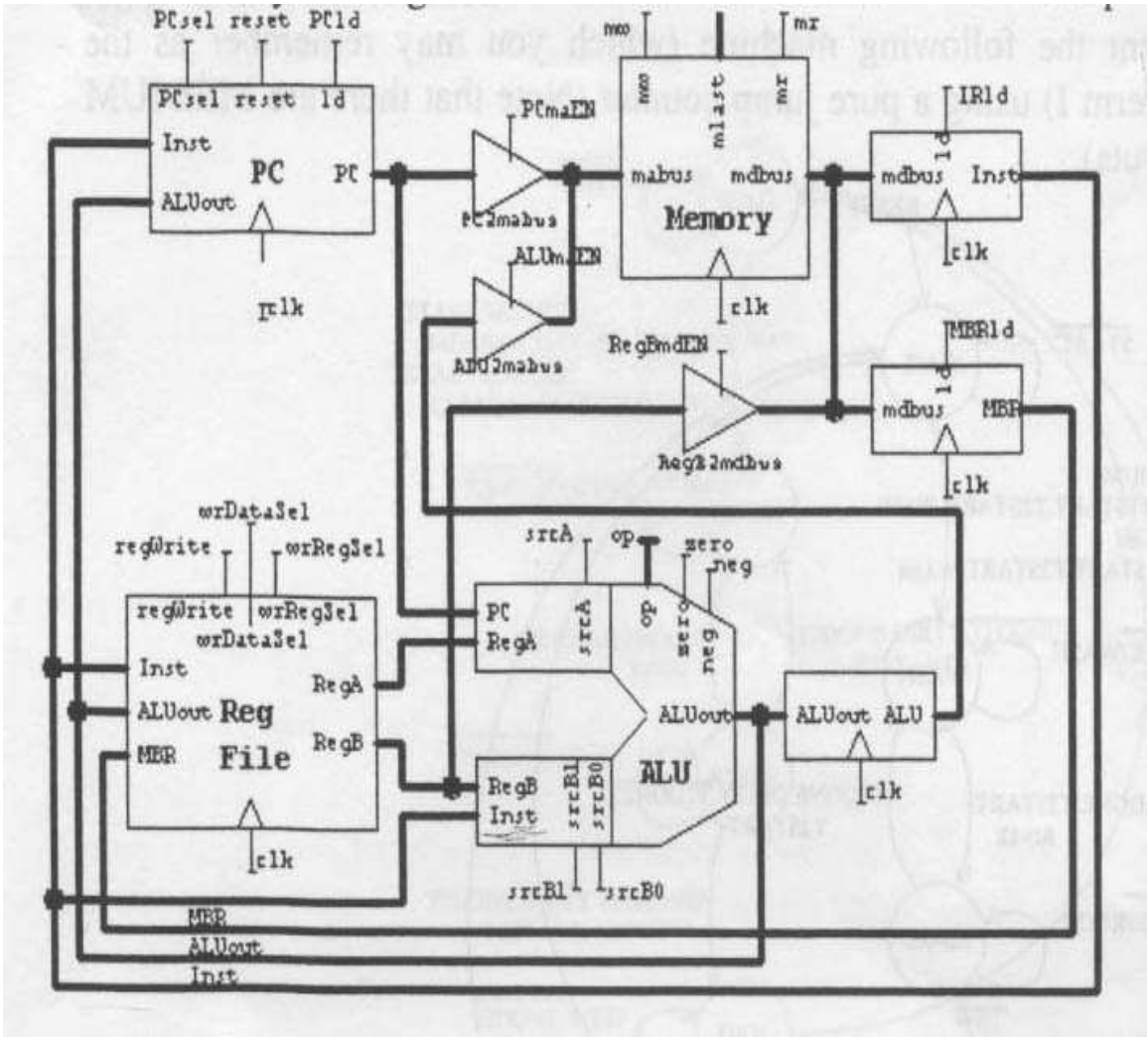
The easiest way to perform arithmetic operations using the sign-and-magnitude system is to convert to 2's complement for your calculations. You are given the following components:
- A 4-bit universal shift register
- As many 1-bit full adders as you need
- As many 2-input XOR gates as you need
- AS many 2-input NAND gates as you need

a) Design a circuit to convert a 4-bit sign-and-magnitude number of 2's complement number.

b) Design a circuit to convert a 4-bit 2's complement to a sign-and-magnitude number.

**Problem 3**

Trace the execution of the current instruction in the following microprocessor datapath. The instruction syntax is given on slide 22 of the class notes on computer organization.



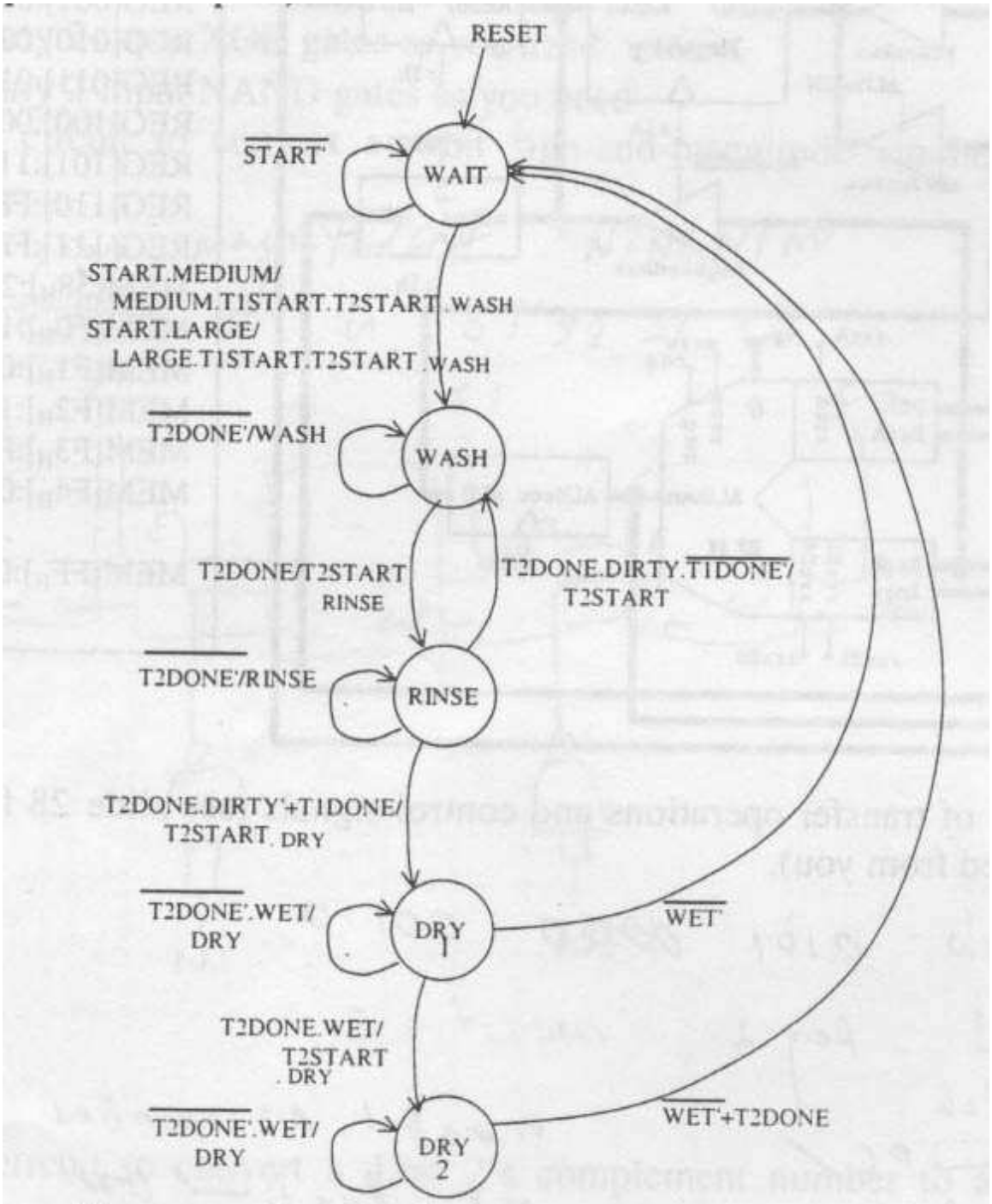
a) List the sequence of transfer operations and control signals (see slide 28 for an example of what is expected of you).

b) After the instruction execution is complete, list the contents of the following, in hexadecimal:
PC:
REG[010]:
REG[101]:
REG[000]:
REG[011]:
REG[110]:
REG[001]:
REG[100]:
REG[111]:

c) Suppose you want to display the result of the execution of your instruction on the display (which is connected to MEM[FFH]. Write the contents of MEM[39H].

**Problem 4**

You are going to implement the following machine (which you may remember as the washing machine from midterm I) using a pure jump counter (Note that there are MEDIUM and LARGE inputs and outputs).



a) Determine an optimal encoding for the states.
WAIT:
RINSE:
WASH:
DRY1:

b) Determine the control functions:

CNT =

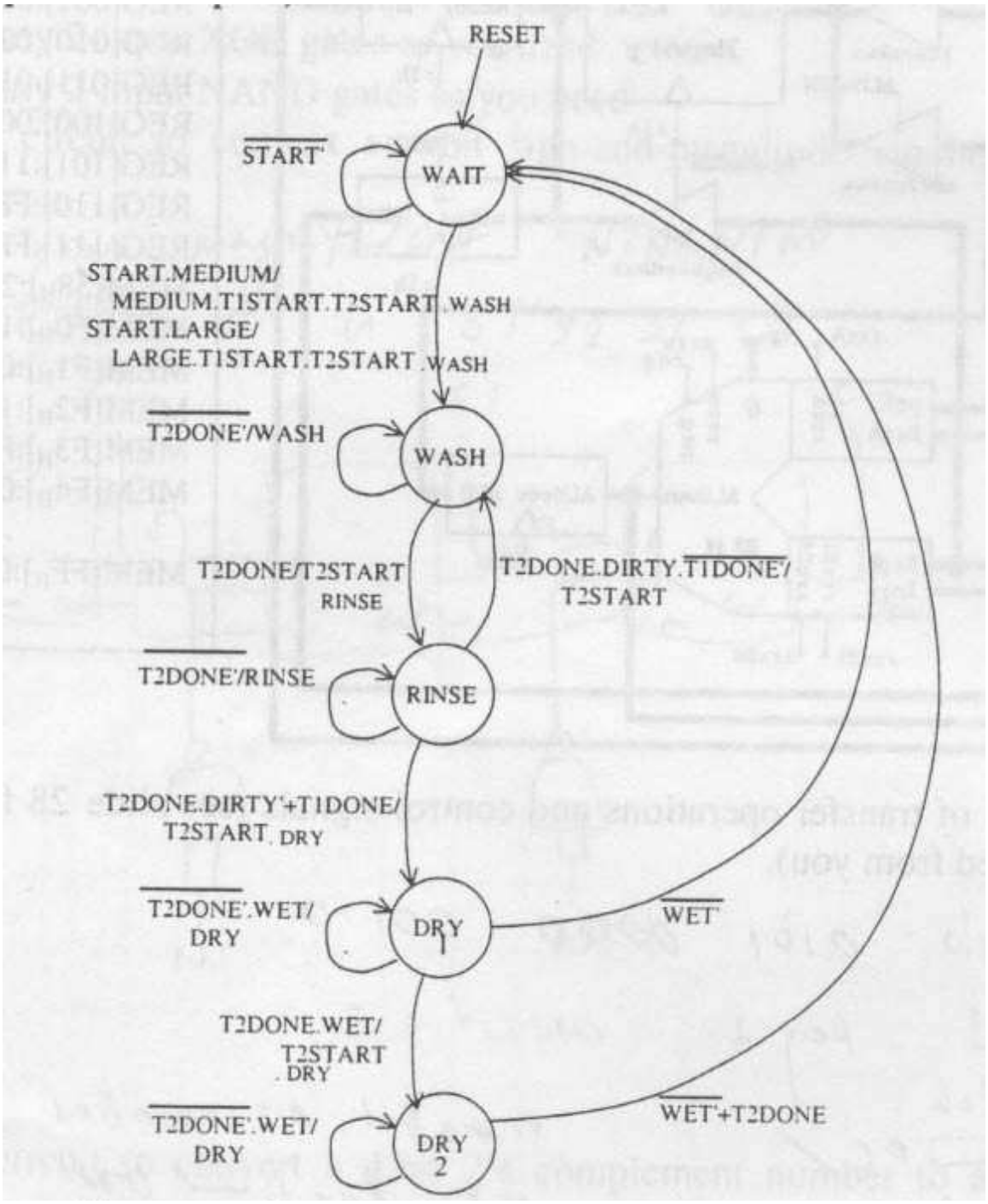
LD =

CLR =

c) List the contents of the Jump ROM

**Problem 5**

You are going to re-implement the washing machine controller from the previous problem using vertial mericode.



a) List all sets of mutually exclusive outputs

b) Assuming you use 1-hot encoding for all non-mutually exclusive output groupings, what is the minimum number of bits to encode the outputs?

c) Assum you need a 5-bit ROM address to encode the machine. Write out the format (as on slide 39 of the controller implementation notes) of RT and BJ instructions for this machine assuming (b).

d) List the output functions:

LARGE =

MEDIUM =

T1START =

T2START =

WASH =

RINSE =

DRY =

e) Draw a circuit diagram for the jump counter. You need to show the output function implementations. Use the PLA below to implement your control functions, and use a 74163 4-bit counter as the state storage element.