Computer Science 152, Spring 1994
Midterm #2
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This is a *closed-book, closed-note, no calculator* exam. You have 90 minutes.

You might not have time to complete all the questions, so read all of them first.

Each question is marked with it's number of points (one point per expected minute of time).

Show your work. Write neatly and be well organized.

Good luck!

1. Short Answer [10 pts]

a. True or False: In an n-way set associative cache scheme, n must always be a power of 2.
b. True or False: To properly handle an external interrupt, the current instruction must be suspended then restarted.
c. Why can hard disks store a higher data density than floppy disks?
d. True or False: Asynchronous busses are popular because they can operate at a higher data rate.
e. True or False: TLB misses always generate CPU interrupts.
f. True or False: In CMOS, ROMs can be implemented with PLA circuits.
g. What is the rotational delay for a disk rotating at 5000 rpm?
h. List two ways to deal with large translation tables in a page's virtual memory system.
i. Why is dynamic RAM denser than static RAM?
j. What is the main advantage of a microprogrammed (multi-cycle) processor design over a non-pipelined single-cycle design?

2. Caches [10 pts]

Consider the configuration shown below with a CPU, an instruction cache (Icache), and a main memory. The CPU has a 10ns clock cycle and 32-bit instructions. Icache hits take 10ns. The main memory must be implemented using 120ns access time 1Mbit X 1bit DRAM parts and must be exactly 4 MBytes. The CPU is pipelined with a cycle time of 10 ns.

CPU	<----------	Icache	<----------	Main Memory
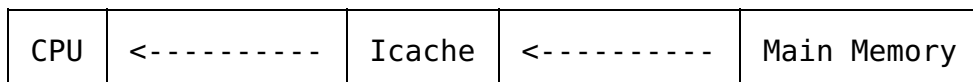
a. Sketch the organization of the main memory.
b. Assuming we would like to make maximum use of the main meory-Icache bandwidth, what is the minimum hit rate that the Icache must provide in order to minimize processor stalls due to Icache misses?

3. Super-pipelining [10 pts]

Consider a pipelined processor with more stages than the usual RISC processor. In this processor the instruction and data caches and the ALU are all split into two stages. All other stages are as in our usual pipeline design.

   a. What is the theoretical maximum speed-up for ths processor over a single cycle processor design? What is the speed-up over the standard pipeline?
   b. List all the factors that will contribute to prevent reaching the theoretical speedup.
   c. Assume this design uses delay slots and forwarding to deal woth data control hazards, how many load delay slots are needed? How about branch delay slots? Are there any other delay slots?

4. Virtual Memory [20 pts]

Consider a virtual memory system with 1KByte pages, a fully associative translation look-aside buffer (TLB) with 64 entries, and a single cache with 2KBytes of storage for data and instructions (not counting tags). The cache uses physical addresses. Virtual and physical addresses are 32 bits, and data and instructions are 32 bits each.

Design a system that attempts to minimize memory access times. Sketch your design showing addess translation and caching, cache organization, and the format of the entries in the cahe and TLB.

5. Input/Output [10 pts]

Most machines today have a dual-ported frame buffer holding the bit-map for the display device. Consider the feasibility of using single-ported memory and of sharing the processor/memory bus with the display device. In our system the processor and bus cycle at 60MHz. Assume we have a 512 bit wide main memory, bus, and 512 bit cahe blocks. Main memory accesses take 50ns.

   a. For a 1000 pixel by 1000 pixel color display, with 24 bits of color and 60Hz refresh, what is the fraction of the memory bandwidth that would be required by the display?
   b. For our set of applications only 256 colors are ever used on the screen at one time. How could we reduce the memory bandwidth needed for the screen update?
   c. Now what is the fraction of the memory bandwidth used ny the display?

6. Processor Design [30 pts]

You are to design a pipelined processor with the same instruction set as the MIPS but implemented with a simple two stage pipeline. The first phase of the pipeline, called "I" includes instruction fetch (40ns), instruction decode, and register read (20ns), and the first half of the ALU operation (20ns). The second phase called "X" includes the second half of the ALU operation (20ns), memory access (40ns), and register write (20ns). There are separate memory ports for instructions and data with no caches. Your design must have no load or branch delay slots and no stalls.

   a. Draw a pipeline diagram illustrating the overlap of several instructions and the timing within each phase. Draw arcs to illustrate any potential data or control hazards.
   b. Draw an RTL level diagram for the processor. Show all necessary functional blocks, register, busses, and control blocks. The control logic does not have be shown in detail.