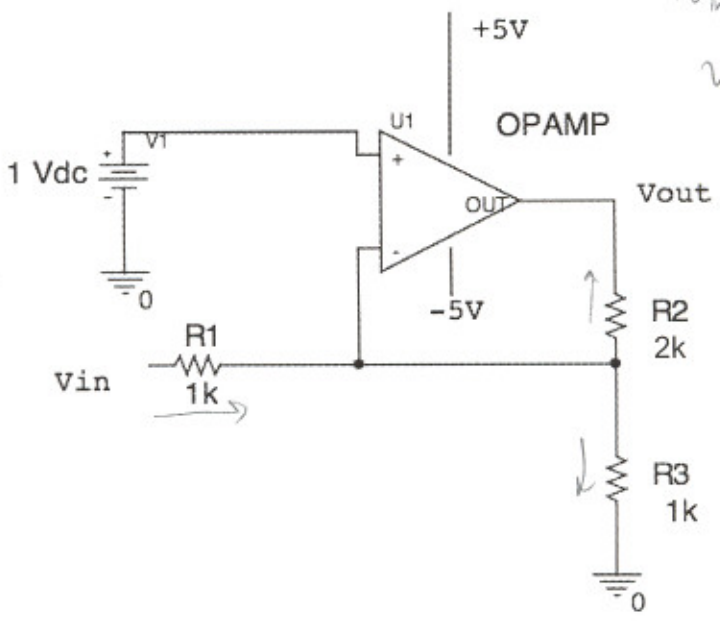
$\frac{V_{in}-V^+}{1k} = \frac{V^+}{1k} + \frac{V^+-V_{out}}{2k}$

$V_{in} = V^+\left(1+\frac{1}{1+\frac{1}{2}}\right) - \frac{1}{2}V_{out}$

$V_{out} = -2V_{in} + 5V^+$

Problem 1 ~~(22 points)~~



check if $V_{in}=1V$

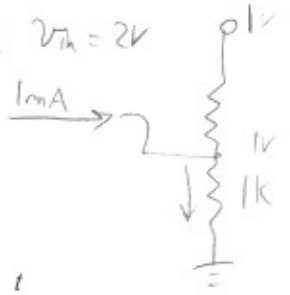
$V_{out}=3V$

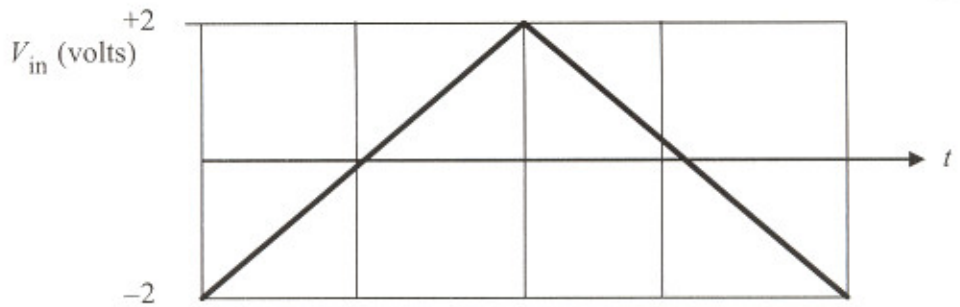
$3V \cdot \frac{1}{3} = 1V$ ✓

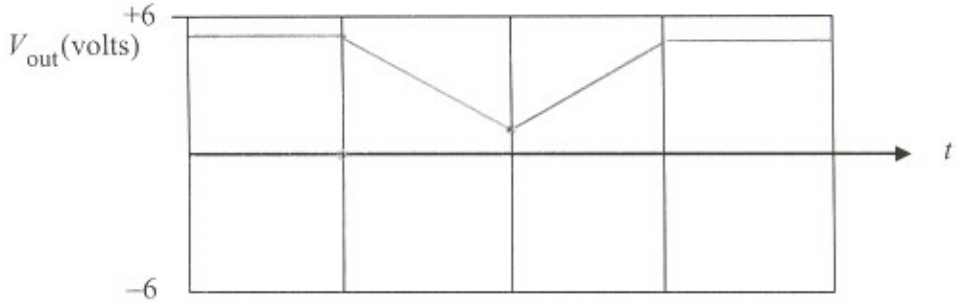
V_{in}	V_{out}
-2	9 → 5
-1	7 → 5
0	5
1	3
2	1

Given V_{in}, sketch V_{out}.

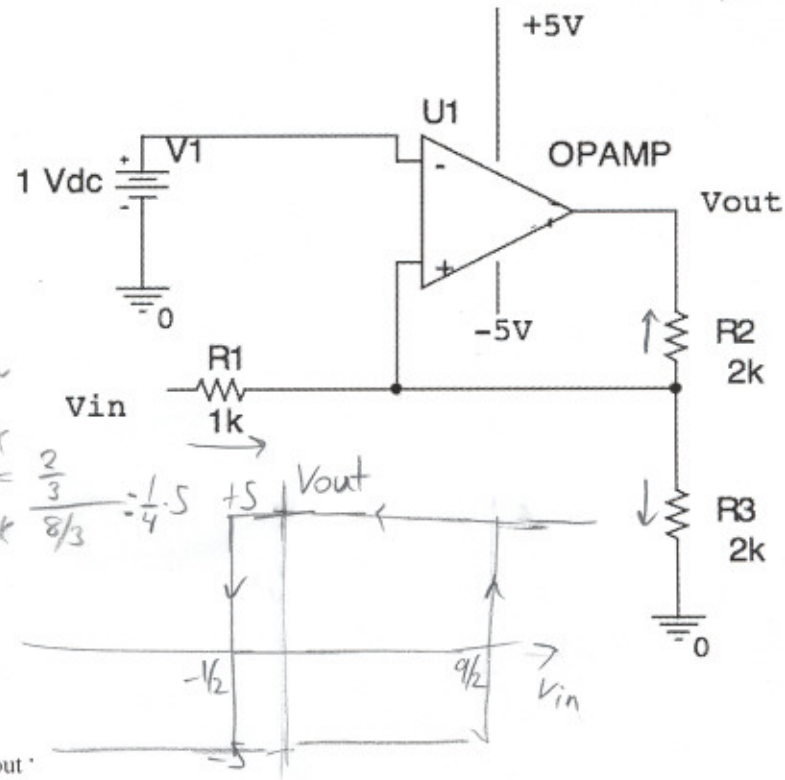
check $V_{in}=2V$



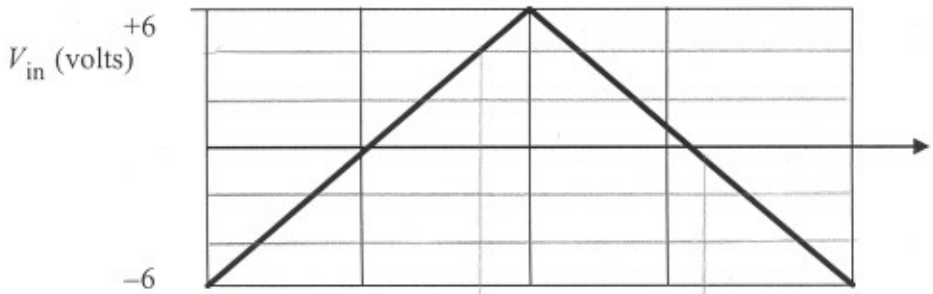


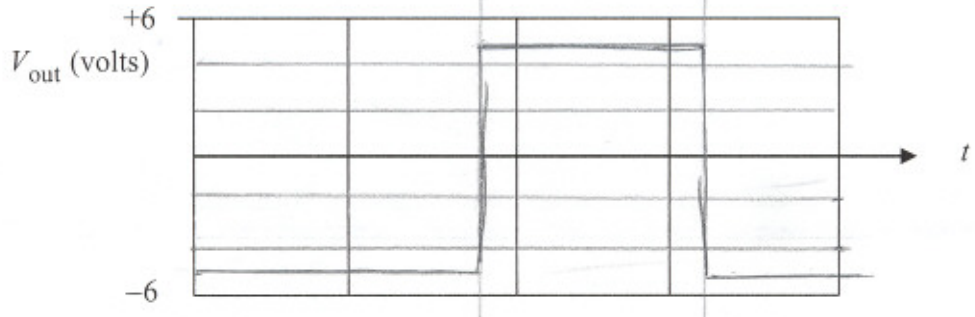


Problem 2 ~~(22 points)~~



Given V_{in}, sketch V_{out}.





positive feedback.

Case #1 Vout = +5V

$v^+ > 1V$ since $V_{out} = A(v^+ - v^-)$

$\frac{v_{in} - v^+}{1k} = \frac{v^+}{2k} + \frac{v^+ - v_{out}}{2k}$

$2v_{in} = v^+(2+1+1) - v_{out}$

$v^+ = \frac{2v_{in} + v_{out}}{4}$

$= \left(\frac{1}{2}v_{in} + \frac{5}{4}\right) > 1$

$\frac{1}{2}v_{in} > -1/4$

$v_{in} > -\frac{1}{2}V$

Case #2, Vout = -5V

$v^+ < 1V$ since $V_{out} = A(v^+ - v^-)$

$v^+ = \frac{1}{2}v_{in} - \frac{5}{4}$

$= \frac{1}{2}v_{in} - \frac{5}{4} < 1V$

$\frac{1}{2}v_{in} < \frac{9}{4}$

$v_{in} < \frac{9}{2} = 4\frac{1}{2}$

Vout = 5

Vin	v+
0	5/4

9/2

2k

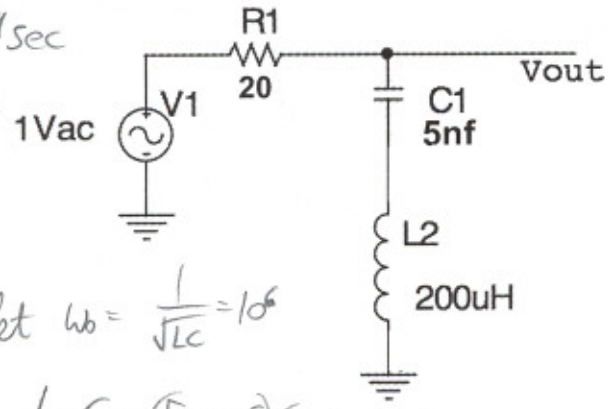
V+ = 2/3 = 1/4 · 5 = +5 Vout

1k 2k 8/3

-1/2 9/2 Vin

-5

Problem 2 – (?? points)



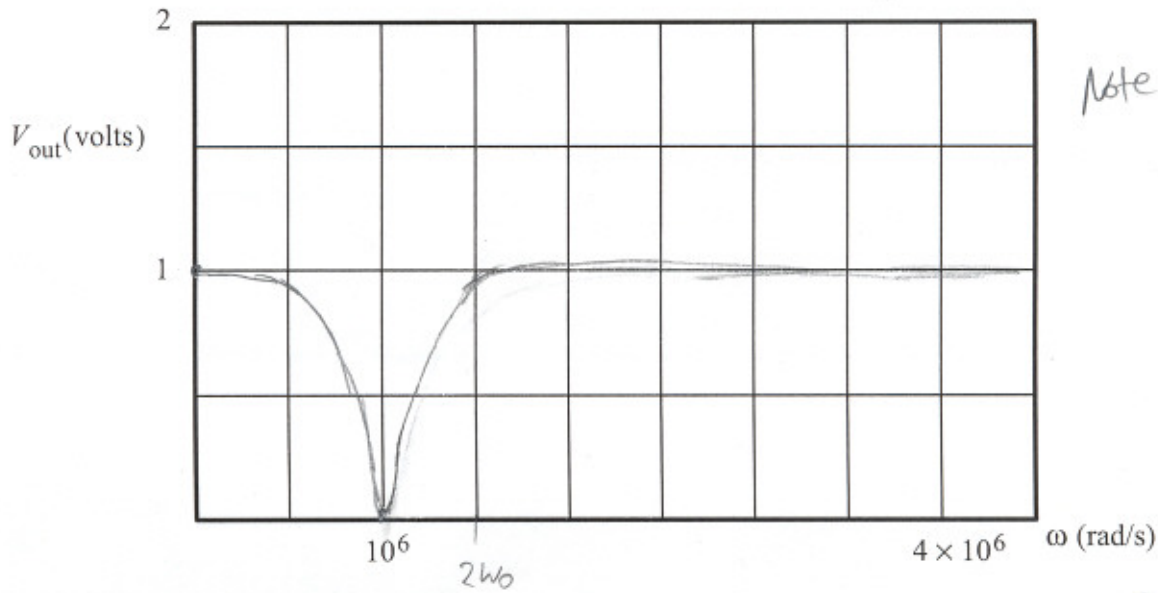
In this problem, $v_1(t) = cos(\omega t)$.

[0 pts.] **a)** What is $|v_{out}(t)|$ for $\omega = 0$?

[0 pts.] **b)** What is $|v_{out}(t)|$ for $\omega = 10^6$ rad/s?

[0 pts.] **c)** What is $|v_{out}(t)|$ for ω very large?

[0 pts.] **d)** Sketch the magnitude response for V_{out} as a function of ω.



610 – 617

Problem 3 – (?? points)

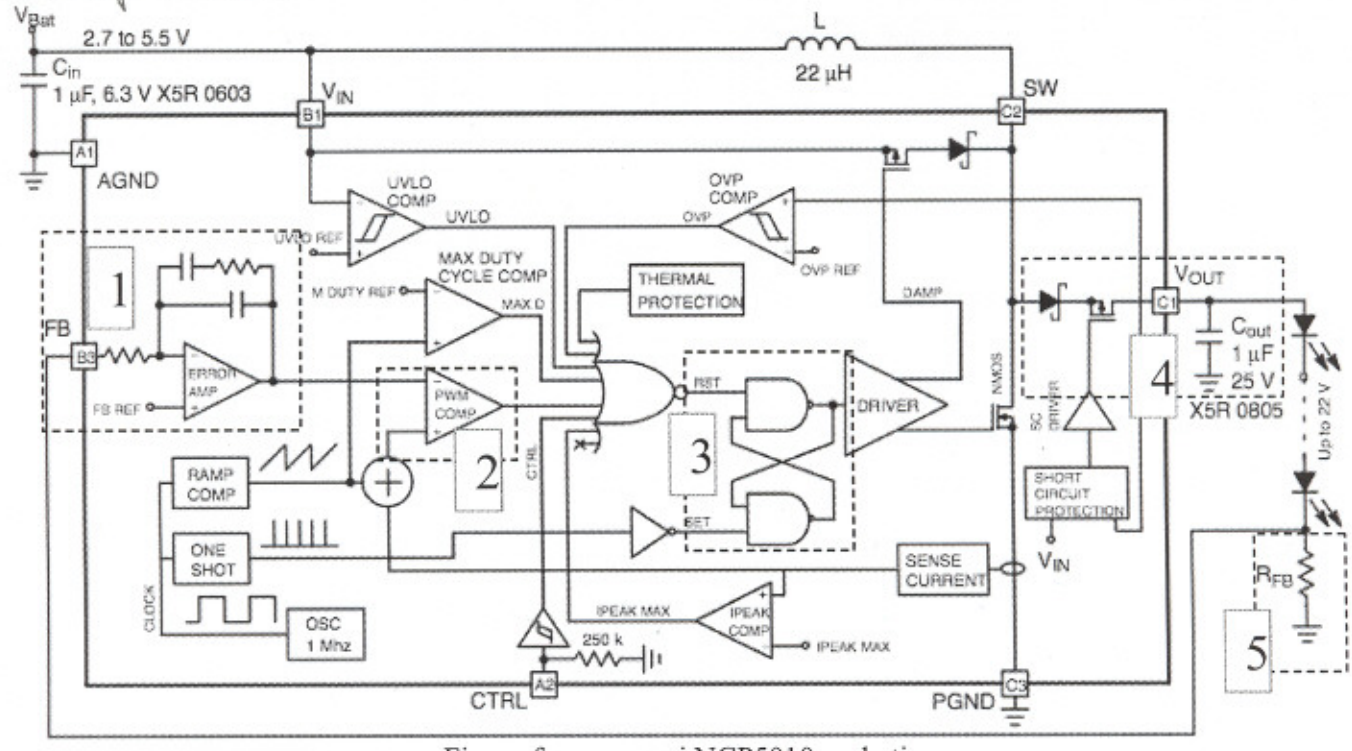


Figure from onsemi NCP5010 verbatim

The power supply circuit above uses a transient response on an inductor L (at top) to convert from an input voltage V_{Bat} to an output voltage up to 22 volts to drive a chain of LEDs. This power supply circuit runs at 1 MHz, and provides a DC output. The diode symbol with the squiggle is a Schottky diode, which works like a silicon diode except $V_{\text{on}} = 0.3$ volts. Abbreviations: FB=feedback, SW=switch, AGND=PGND=ground, CTRL=control. **RON: WHAT IS ⊕ ?**

1 **[0 pts.] a)** The circuit labelled 1 looks similar to a familiar op-amp circuit. What type of circuit is this?
integrator with level set and high frequency feedback mult

1 **[0 pts.] b)** The circuit block labelled 2 looks similar to a familiar op-amp circuit. What type of circuit is this?
Comparator

1 **[0 pts.] c)** In circuit block 4, what would the gate voltage of the PMOSFET be to have current flow from SW to V_{out}? 0 so $V_{GS} \approx -V_{OUT}$

2 **[0 pts.] d)** In circuit block 4, what is the function of the diode and capacitor C_{out}?
rectifier and filter capacitor to convert AC to DC.

1 **[0 pts.] e)** The circuit block labelled 3 looks similar to a familiar digital circuit. What type of circuit is this?
latch or unclocked flip flop.

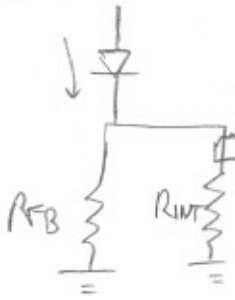
Problem 4 (Cont.)

2 **[10 pts.] f)** Should the CTRL input be at high or low for the power supply to be working?

if RST is low (0) latch can never set. This CTRL needs to be low so that NOR output can go high when all inputs are low.

2 **[0 pts.] g)** Typically R_{FB} (block 5) would be a very small value compared to the resistor on the op-amp input in circuit block 1. What does the voltage across R_{FB} tell the circuit about the chain of LEDs?

Voltage across R_{FB} is proportional to current through LED chain. $V = i_{LED} R_{FB}$

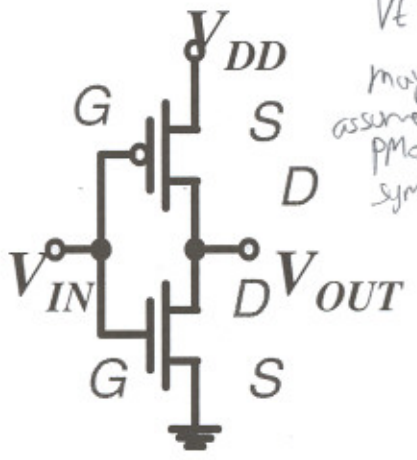


– input of error amp is at virtual ground.

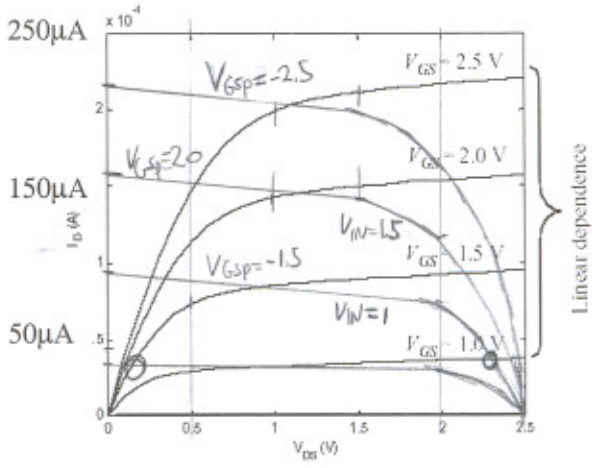
Current divider $R_{FB} << R_{INT}$ so current goes through R_{FB}.

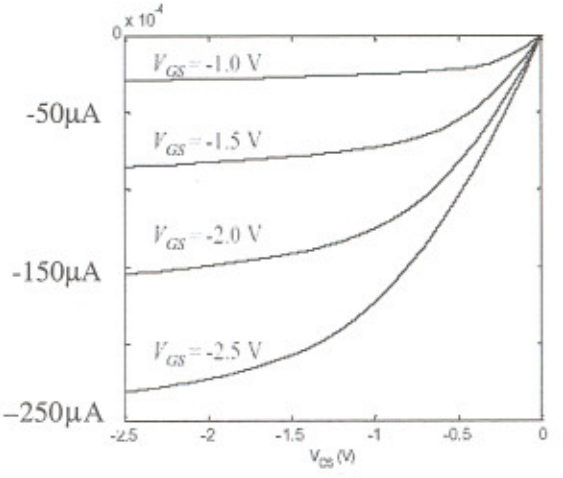
Problem 4 – (12 points) Key

Accurately sketch V_{out} vs. V_{in} for the CMOS circuits shown below. Let V_{DD} = 2.5 V.



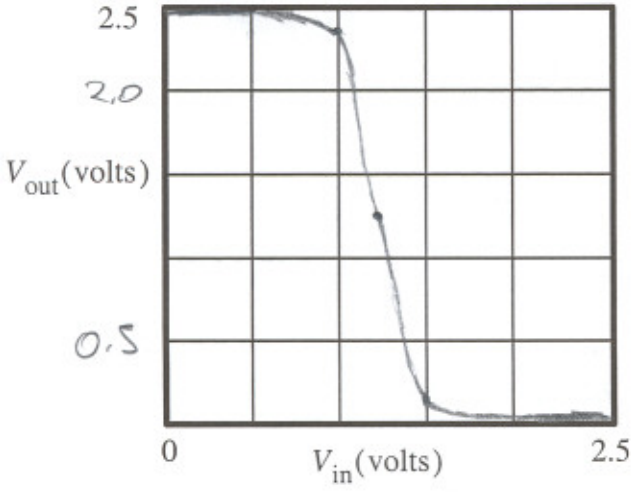
V_t not given
maybe 0.5V?
assume
pMos & NMOS
symmetric





V_{in}	V_{GSn}	V_{GSp}	I_D	V_{DS}
0	0	-2.5	0	2.5
0.5	0.5	-2	~0	2.5
1.0	1.0	-1.5	40µA	2.3V
1.5	1.5	-1.0	40µA	0.2V
2.0	2.0	-0.5	~0	0
2.5	2.5	0	0	0
1.25	1.25	-1.25	50µA	1.25V

CMOS



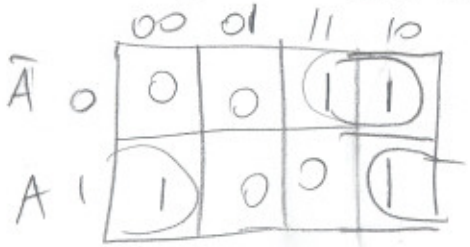
Problem 5 – Logic Questions (?? Points) 6:45 – 7:05

[0 pts.] a) It is good practice to simplify logic functions before making IC chips to realize them. Why?

Reduce # of transistors used and hence area and power.
Also reduces cost.

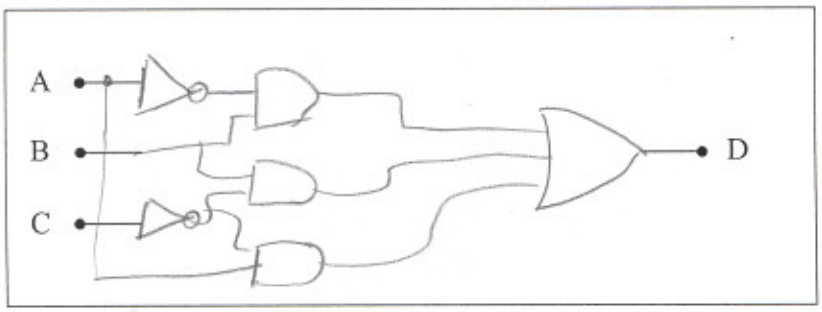
[0 pts.] b) Here's a logic function, F, of three variables A, B, and C that might represent some real-world situation. Simplify the function, if it's possible, using either of the two methods that we described in class and on the homework. Make your method clear to the grader.

$\bar{A}BC + A\bar{C} + B\bar{C} = F$



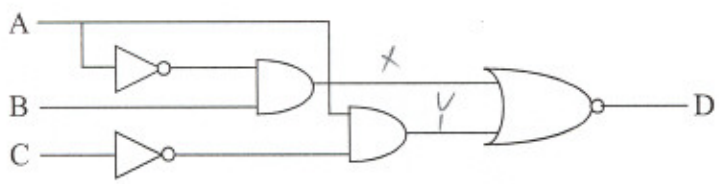
$D = \bar{A} \cdot B + A\bar{C}$

[0 pts.] c) Draw a circuit of logic gates to realize the simplified logic function and fill in the truth table.



A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

[0 pts.] d) Here's a circuit for some logic function. Write a sum-of-products expression for the function.



$D = \bar{A} \cdot \bar{B} + A \cdot C$

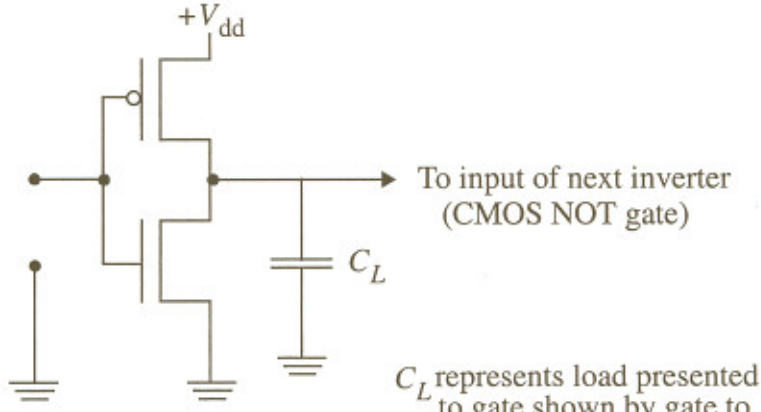
A	B	C	D	X	Y
0	0	0	1	0	0
	0	1	1	0	0
	1	0	0	1	0
	1	1	0	1	0
1	0	0	0	0	1
	0	1	1	0	0
	1	0	0	0	1
	1	1	1	0	0

Problem 5 (Cont.)

[2 pts.] **e)** If each gate in the circuit of Part d), above, has the same unit delay of 50 ps, what is the minimum time before the correct output appears at D, assuming that the values of A, B, and C all appear at time $t = 0$?

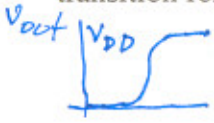
Longest path from inputs (A, B, C) to output (D) goes through 3 gates → 150ps

[6 pts.] **f)** The CMOS circuit for a NOT gate is shown:



This gate drives the input of an identical NOT gate. Suppose the resistance of a p-channel is 10kΩ, the resistance of an n-channel is 5kΩ, and the total gate-to-source capacitance C_L is 20 fF.

(2 pts.) **i)** What is the value of the RC product that is used in finding the time delay of the low-to-high transition for the NOT gate?



C_L charges through PMOS → RC product is $R_p C_L = 10\,k\Omega \cdot 20\,fF = 2\times10^{-10}\,s = 0.2\,ns$

(2 pts.) **ii)** What is the value of the RC product that is used in finding the time delay of the high-to-low transition for the NOT gate?

C_L discharges through NMOS → RC product is $R_n C_L = 5\,k\Omega \cdot 20\,fF = 1\times10^{-10}\,s = 0.1\,us$

(4 pts.) **iii)** Given that $e^{-0.69} = \frac{1}{2}$, determine the gate propagation delay when the gate input goes from 0 to V_{DD} and back again.

Total delay is $\tau_{L-H} + \tau_{H-L}$ where τ's are times after input changes until output falls or rises to $V_{DD}/2$. $t_{L-H} = 0.69 R_p C_L$ & $t_{H-L} = 0.69 R_n C_L$.

Total time $= t_{L-H} + t_{H-L} = 0.69[R_p C_L + R_n C_L]$

$= 0.69\,[2\times10^{-10} + 1\times10^{-10}] = 3\times0.69\times10^{-10}$

$\approx 2.1\times10^{-10}\,s$

Problem 7 – Transient Problem (?? points)

Consider a traffic light in which the yellow (caution) light is a group of LEDs wired together, and suppose that when used, the yellow light is on for 5 seconds. Suppose further that all these LEDs operate at 1.6 volts and that the total current they draw is 100 mA.

[0 pts.] a) What is the resistance, R_{LED}, of this group of LEDs?

$R = \frac{V}{I} = \frac{1.6V}{100mA} = 16\Omega$

[0 pts.] b) What is the peak power, P, dissipated by these LEDs?

$0.16 watt = (1.6)(0A)$

[0 pts.] c) How much energy is consumed by the yellow light in one cycle of operation (one cycle means transition from green, to yellow, to red lights)?

$(5sec)(0.16W) = 0.8 jole$

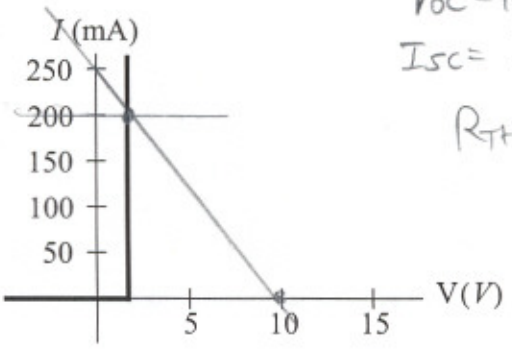
[0 pts.] d) Suppose that this energy you found in Part c), above, is supplied each cycle by a capacitor, C, initially charged to 10 volts. What value of C do you need?

$W = \frac{1}{2}CV^2, \quad \frac{2(0.8)}{10^2} = \frac{1.6}{6^2} = C, \quad C = 1.6 \times 10^{-2} F$

[0 pts.] e) You need to put a resistor in series with an LED and its voltage source. Why?

To keep current banded and LED from burning up.

[0 pts.] f) Find the approximate resistance, R_{series}, to put in series with a 10-volt battery ($R_{internal} = 0.1\Omega$) so that the current through the LED is no more than 200 mA. Assume that the group of LEDs has the I-V characteristic shown here:



$V_{OC} = 10V$

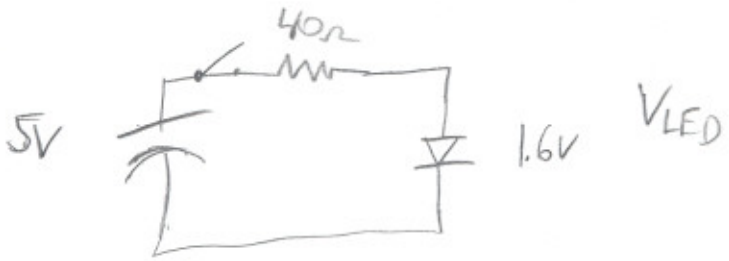
$I_{SC} = 250mA$

$R_{TH} = \frac{V_{OC}}{I_{SC}} = \frac{10V}{0.25} = 40\Omega$

8 of 12

Problem 4 (Cont.)

[0 pts.] **g)** A student from EE42/100, just hired by Berkeley's Traffic Division, suggests running the yellow light from a capacitor connected in series with R_{series}, and a circuit that recharges the capacitor to 5 V just before each yellow light usage. An experienced traffic engineer thinks this is not a good approach. Why?



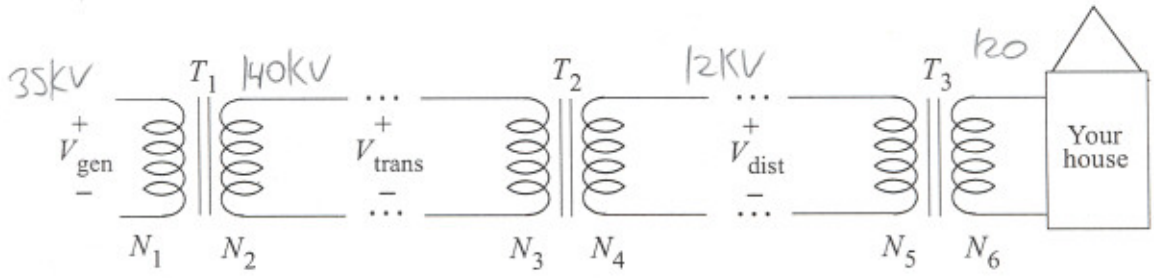
$\frac{5V - 1.6V}{40\Omega} = \frac{3.4}{40\Omega}$ < 100mA, not bright enough, even with bigger capacitor.

Also light intensity will be fading

7

Problem ~~8~~ – Phasor Problem (?? points)

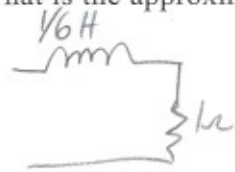
The sketch below represents part of the AC power supply system in the U.S. At the source (Bonneville Dam in Oregon) the generators driven by falling water from a dam are rated at 35 kV. The voltage is stepped up to 140 kV for transmission to Berkeley, where the voltage is reduced to 12 kV for distribution around the city, and then reduced again to 120 volts by a transformer just outside your house.



[0 pts.] **a)** For transformer T1, if the primary winding has 20 turns, what is the number of turns on the secondary? 80

[0 pts.] **b)** Suppose you have in your garage a Bridgeport milling machine whose electric motor can be modeled as a one-sixth H inductor in series with a 1Ω resistor. What is the approximate value of the inductive impedance at PGE's 60 Hz frequency?

$Z = j\omega L = j\left(2\pi \cdot 60 \cdot \frac{1}{6}\right) = j20\pi\ \Omega$



[0 pts.] **c)** Using the same parameters as in b), above, what is the approximate impedance (in A + jB form) of the series combination of the inductor and the resistor?

$1 + j20\pi\ \Omega \approx 1 + j125\ \Omega$

[0 pts.] **d)** Again using the same parameters as in b), above, which of the following is correct? (Checkmark correct answer.)

- **i)** The phase angle of the impedance is approximately zero.
- ✓ **ii)** The phase angle of the impedance is almost +90°.
- **iii)** The phase angle of the impedance is almost −90°.

[0 pts.] **e)** Once again using the same parameters as in b), above, what is the approximate value of the reactive power drawn under these conditions?

$Q = V_{RMS} I_{RMS} \sin\theta$

$= 120 \cdot \frac{120}{20\pi} \cdot 1 = \frac{720}{\pi}$ VAR

Real $\frac{1}{2}\mathrm{Re}\{VI^*\}$ Im $\frac{1}{2}\mathrm{Im}\{VI^*\}$

$I_{RMS} = \frac{V_{RMS}}{\omega L}$

[0 pts.] **f)** Again using the same parameters as in b), above, what might you (or, in fact, the power company) do in order to reduce the amount of reactive power you are drawing?

Add capacitance in parallel to cancel out inductive reactance.

Problem 8 – Short Questions (12 points) KEY

Note: If in answering any of these questions you feel you are making a special assumption that you want the grader to know about, please mark that question with a big asterisk (*) in the right-hand margin and explain on the back of the page.

(A) True/False

[1 pts.] **a)** T ___ F X At very low frequency, a capacitor behaves like a short circuit.

[1 pts.] **b)** T ___ F X You can use the superposition analysis technique on any nonlinear circuit.

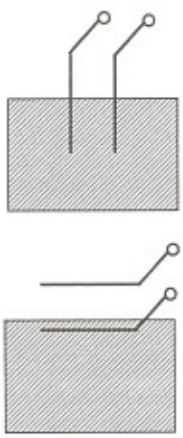
[1 pts.] **c)** T X F ___ One step in superposition analysis is to turn off all voltage sources, meaning to set all voltage sources to 0 volts.

[1 pts.] **d)** T X F ___ One way to make p-type silicon is to diffuse into the silicon acceptor atoms from group III of the periodic table, so that they ionize thermally and can then move freely through the silicon lattice.

[1 pts.] **e)** T X F ___ If you put an inductor in series with a capacitor, at some frequency the impedance of the combination will equal zero.

[1 pts.] **f)** T X F ___ If you put an inductor in parallel with a capacitor, the frequency ω_r, where $\omega_r^2 LC = 1$, is the frequency at which the imaginary part of the inductor impedance is the negative of the capacitor impedance.

[1 pts.] **g)** One electronic application that was the basis of a homework problem involved a capacitor formed by two parallel conducting plates stuck into a tank partially filled with a dielectric liquid (see upper sketch at right). A student in our class asked what would happen in a practical case – such as trying to measure water level in a tank being carried in a truck on a rough road, if a thin film of the water happened to cover one of the electrodes, while the other electrode was in the air above the water (see lower sketch at right):



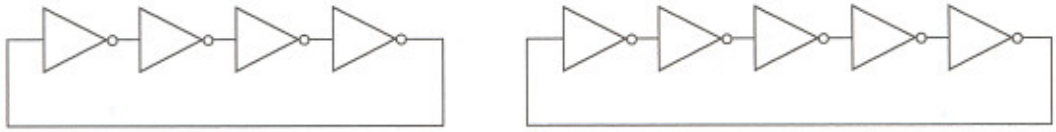
T ___ F X You could model this as being two capacitors in parallel, one being water filled and one being air filled.

Problem 8 (Cont.)

(B) Ring oscillator

When an engineer makes a circuit, such as a novel inverter gate that is faster than any previous circuit, she often determines the circuit's speed by connecting a number of these gates in series and measuring the time it takes a signal to travel around the ring.

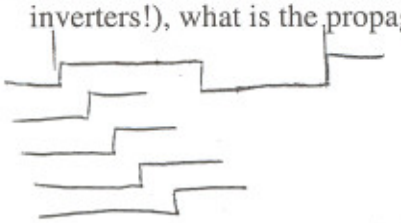
Here are two ring oscillators, one with 4 inverters and the other with 5.



[1 pts.] **a)** Which circuit should she use? Explain why.

4 inverters = latch, 5 inverters = oscillator

[1 pts.] **b)** If the frequency of oscillation of the correct ring oscillator is 500 terahertz (these are very fast inverters!), what is the propagation delay of a single inverter?



$T = 5(t_{PLH} + t_{PHL})$

$t_p = 2 \times 10^{-16}$ sec

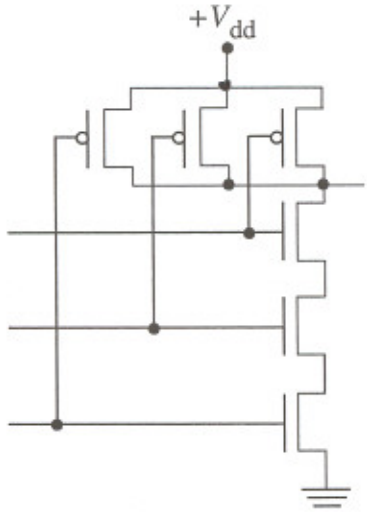
5×10^{14} Hz,

$T = \frac{1}{5 \times 10^{14}} = 2 \times 10^{-15}$ sec

(C) [2 pts.] List at least 4 circuits or devices that you expect contain FETs. (Example: CMOS logic gate. And don't list individual types of logic gates – this sample answer covers all logic gates!)

SRAM, DRAM, class D amplifier, nonvolatile RAM, power-supply/DC-DC converter, MOSFET opamp

(D) [1 pt.] What type of logic gate is this (e.g., OR, transmission gate, etc.)?



3 input NAND gate