UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 130 Midterm #2

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NAME:
SID:

(Close book. One sheet of notes of Chapters 8-18 allowed)

Physical Constants

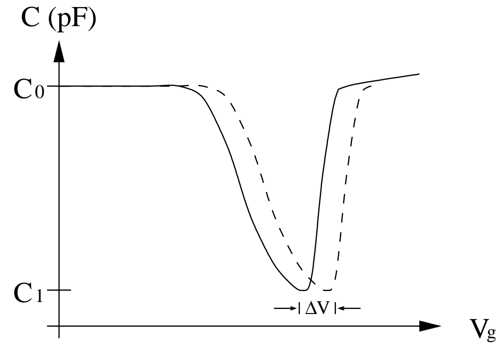
Electronic Charge	q	1.6×10^{-19} C
Permittivity of Vacuum	ε_0	8.85×10^{-14} F/cm
Free Electron Mass	m_0	9.11×10^{-31} kg
Boltzmann's Constant	k	8.62×10^{-5} eV/K

Physical Constants for Si and SiO_2

Si Intrinsic Carrier Concentration	n_i	1×10^{10} cm^{-3}
Si Bandgap	E_{g-Si}	1.12 eV
Si Electron affinity	χ_{Si}	4.05 eV
Diaelectric constant of Si	ε_{Si}	11.7
Dielectric constant of SiO_2	ε_{OX}	3.9

Problem 1	/ 20
Problem 2	/ 24
Problem 3	/ 16
Problem 4	/ 20
Problem 5	/ 20
Total	/ 100

1. (**20 pts**) Consider the C-V curve of a MOS capacitor in the figure (the solid line), the capacitor area is 6400 μm^2. $C_0 = 45\,\text{pF}$, $C_1 = 5.6\,\text{pF}$.



(a) (**3 pts**) What is the substrate type?

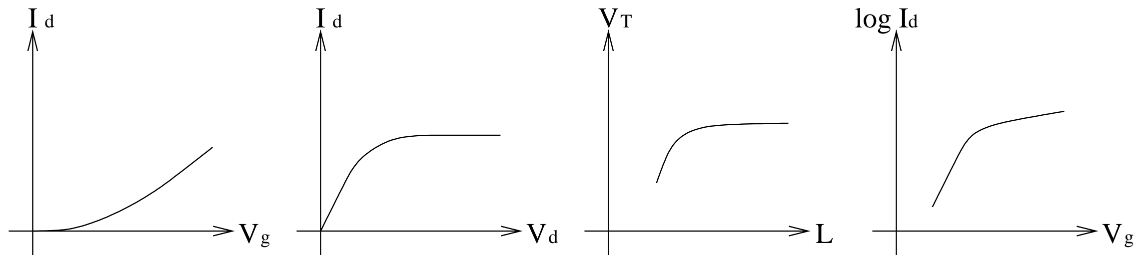
(b) (**5 pts**) Find T_{OX}, the gate oxide thickness.

(c) (**7 pts**) Find the substrate doping concentration N_{SUB}.

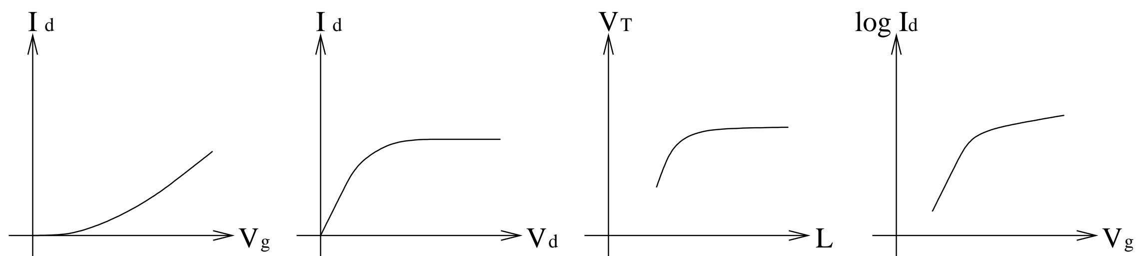
(d) (**5 pts**) If due to oxide fixed charge, the C-V curve shifted from the solid line to the dashied line, with $\Delta V = 0.05\,\text{V}$, what is the type and area density (C/cm^2) of the oxide fixed charge?

2. (**24 pts, 2 pts for each figure**) On each of the following figures, a curve for a MOSFET is given by the solid line. Use a dashed line to qualitatively indicate the new curve that corresponds to the changed condition:

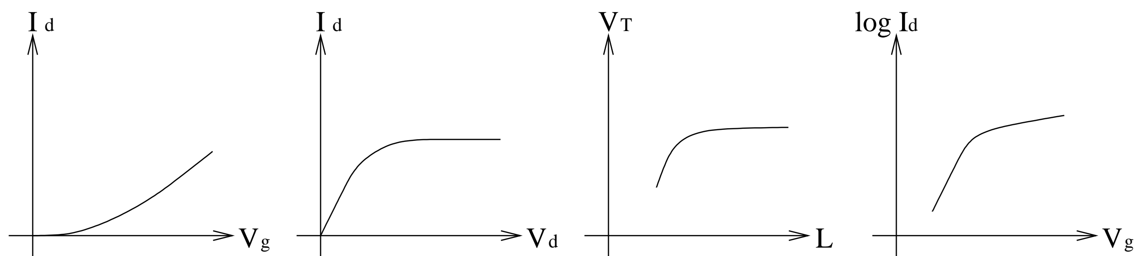
(a) Adding positive charge in the gate oxide:



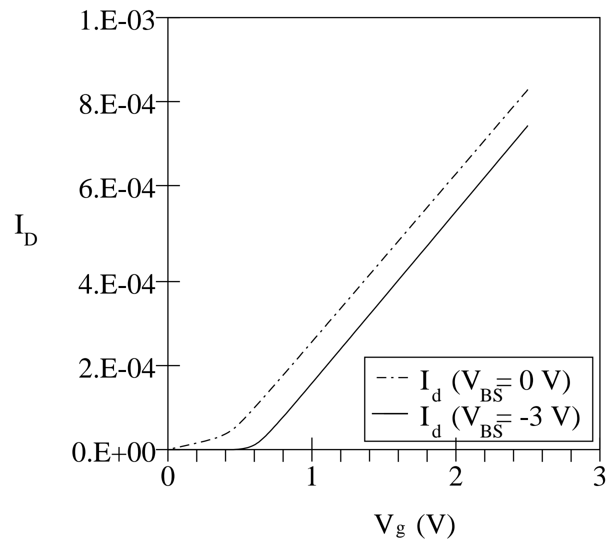
(b) Decreasing N_{SUB}.



(c) Increasing T_{OX}.



3. (**16 pts**) In the following I_D vs. V_g curve, assume $T_{OX} = 50\,\text{A}$ and V_d is small:



(a) (**6 pts**) What is the threshold voltage at $V_{BS} = -3\,\text{V}$?

(b) (**10 pts**) Determine the substrate doping concentration.

4. (**20 pts**) Consider a MOSFET, given $V_T = 0.7\,\mathrm{V}$, $W = 10\,\mu\mathrm{m}$, $L = 0.3\,\mu\mathrm{m}$, $T_{OX} = 50\,\mathrm{A}$ and $I_{DSAT} = 18\,\mathrm{mA}$ at $V_{GS} = 3\,\mathrm{V}$.

   (a) (**8 pts**) Ignoring velocity saturation, find μ_N, estimate I_{DSAT} at $V_{GS} = 2\,\mathrm{V}$.

   (b) (**12 pts**) Now consider the effect of velocity saturation, with $E_{SAT} = 3 \times 10^4\,\mathrm{V/cm}$, use the same μ_N as in part (a), find I_{DSAT} and V_{DSAT} at $V_{GS} = 2\,\mathrm{V}$ and at $V_{GS} = 3\,\mathrm{V}$ respectively.

5. (**20 pts, 4 pts for each question**) Answer each question with one or two sentences.

   (a) What does the term "isolation" mean in CMOS technology? Give the name of one isolation technology.

   (b) Draw the cross-section of the structure produced by LOCOS process.

   (c) Give two reasons why poly-crystalline silicon gate is preferred over metal gate.

   (d) Why is CMOS technology called a low-power technology?

   (e) Why is the sub-threshold current an important parameter in MOSFET design?