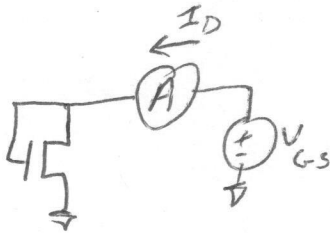


Name _____

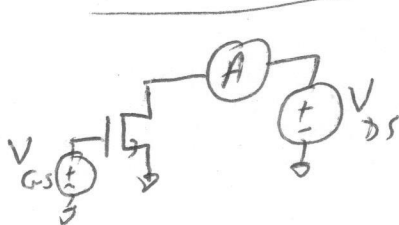
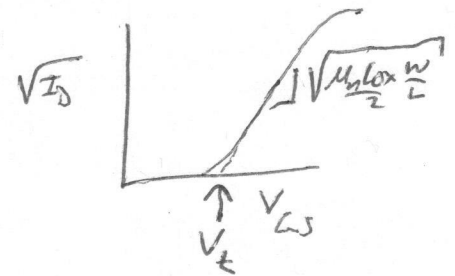
SID _____

Prob.	Score
1+2	/10
3	/12
4	/10
5	/11
6	/13
7	/12
8	/12
9	/12
Total	/

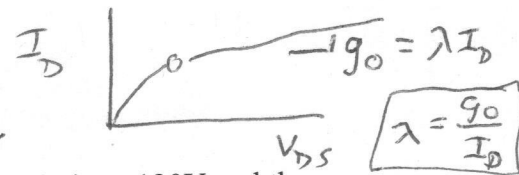
1. [6] You purchased a power NMOSFET and want to verify the DC parameters on the datasheet: V_t , $\mu_n C_{ox}(W/L)$, and λ . Using two voltage sources and a current meter explain exactly what circuit setup you would use, what measurements you would take, and what calculations you would do. Assume that the device is quadratic.



sweep V_{GS} , measure I_D
plot $\sqrt{I_D}$ vs. V_{GS}
slope is $\sqrt{\frac{\mu_n C_{ox} W}{2L}}$
intercept is V_t



pick $V_{GS} > V_t$
sweep V_{DS} , measure I_D ,
plot I_D vs V_{DS}
measure slope g_o



2. [4] Later you bias a similar device with both the gate at 5V and the drain at 120V, and the source grounded, and measure a drain current of 1A. Increasing the gate voltage to 6V increases the current to 2A. With the gate still at 6V, you have to decrease the drain voltage to 20V in order to get the current to drop back to 1A. Near these bias points,

a. What is the transconductance g_m ? $g_m = \frac{1A}{1V} = 1S$

b. What is the output resistance r_o ? $r_o = \frac{100V}{1A} = 100\Omega$

c. What is the channel length modulation parameter λ ? $\lambda = \frac{1}{r_o I_D} = 1/100V$

d. What is the intrinsic gain? 100

3. [12] At $t=0$, the input voltage V_i below transitions from 0 to 2V. The capacitor starts with an initial voltage of 5V. $\mu_n C_{ox} = 200 \mu A/V^2$, $V_t = 1V$, $W/L = 10$. Assume $\lambda = 0$.

a. [1] What is the initial current in the MOSFET immediately after $t=0$?

$$I_D = \frac{200 \mu A}{2} \frac{10 (1V)^2}{V^2} = 1 mA$$

b. [1] What is the initial rate of change of the capacitor voltage?

$$\frac{dV}{dt} = \frac{I}{C} = 10 \frac{9V}{5}$$

c. [1] How long does it take the capacitor voltage to decrease to 1V?

$$4 ns$$

d. [1] What is R_{on} for the MOSFET in the triode region?

$$\frac{1}{\mu_n C_{ox} \frac{W}{L} V_{ov}} = 500 \Omega$$

e. [2] How long does it take the charge on the capacitor to decrease from 0.1V to 0.1mV?

$$\tau = RC = 0.5 ns$$

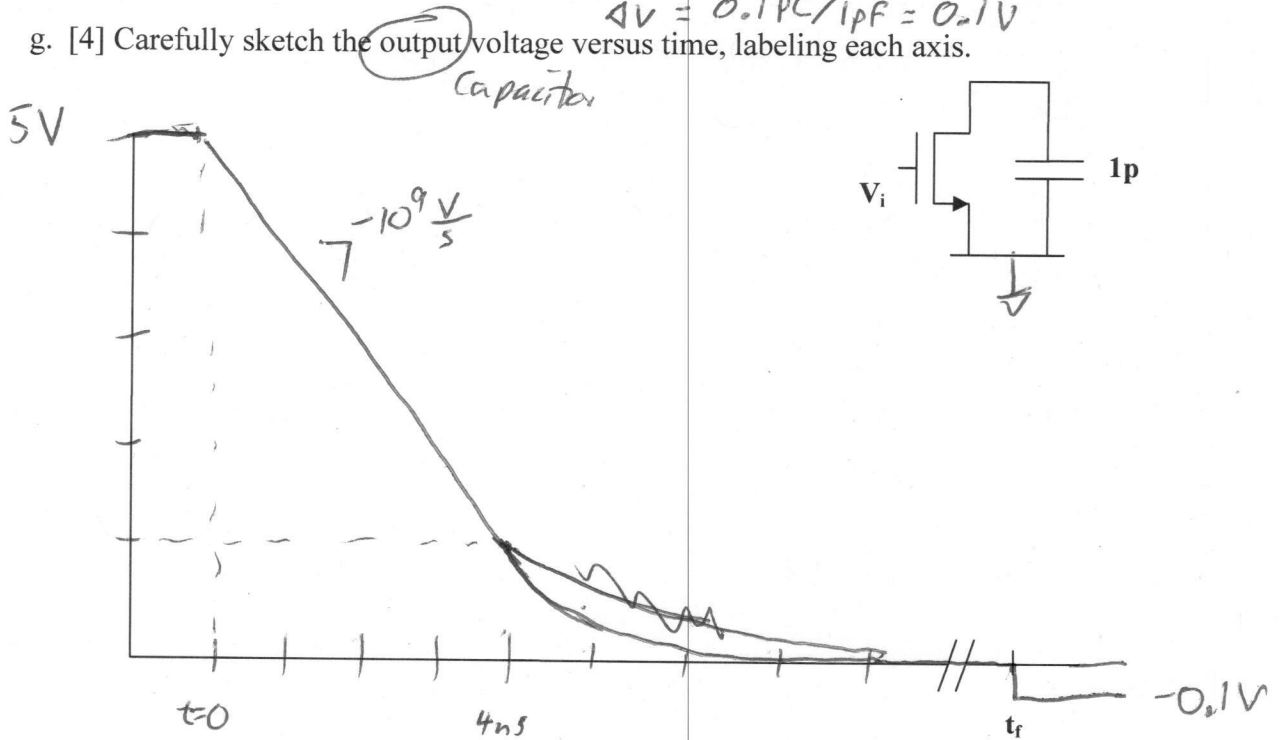
$$0.1\% \Rightarrow 7\tau = 3.5 ns$$

f. [2] If C_{gd} of the MOSFET is 0.1 pF, and at $t=t_f$ that is long compared to the times above the input voltage slowly transitions back to 0, what is the charge injected and the final voltage on the capacitor?

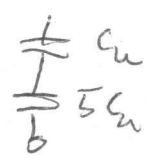
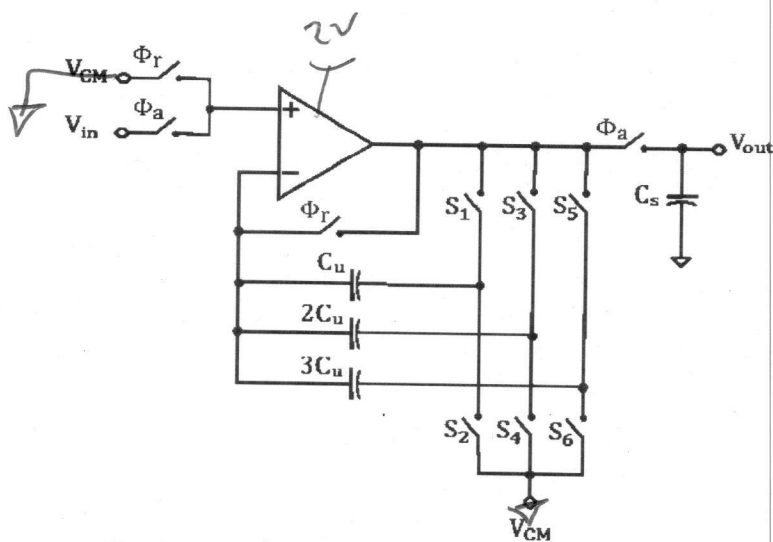
$$C_{gd} V_t = (0.1 pF)(1V) = 0.1 pC$$

$$\Delta V = 0.1 pC / 1 pF = 0.1 V$$

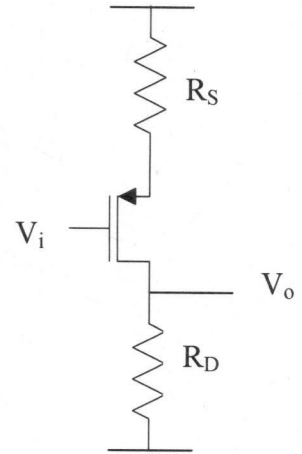
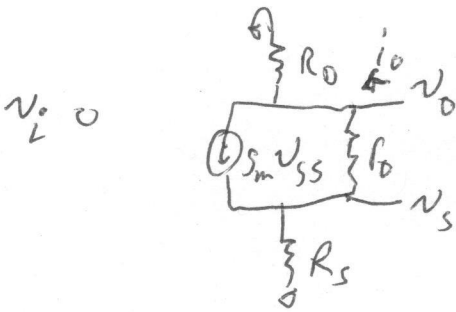
g. [4] Carefully sketch the output voltage versus time, labeling each axis.



4. [10] In the circuit below, assume that $V_{CM} = 0$, and the op-amp is running from a single-sided 2V supply. Assume that Φ_r and Φ_a are non-overlapping clocks.
- [1] during Φ_r , which switches should be closed to ensure that there is no charge on the capacitors, and the op-amp is working normally in unity gain feedback?
 $S_2, 4, 6$ $S_1-5, 6$
 - [2] in Φ_a what is the feedback factor if switches S_1, S_4 , and S_6 are closed (and 2, 3, and 5 remain open)? What is the gain?
 $f = \frac{1}{6}$ $A = 6$
 - [1] If a settling accuracy of 0.1% is required with this switch setting, what is the minimum DC gain necessary for the op-amp?
 $\frac{1}{A_f} = 10^{-3}$ $A = 6,000$
 - [2] With this settling accuracy requirement, and Φ_a phase duration of $1\mu s$, what is the minimum open-loop unity gain bandwidth of the op-amp?
 $2\tau = 1\mu s$ $\tau = 140ns$ $\omega_p = \frac{1}{\tau} = 7Mrad/s$
 $\omega_u = f\omega_p = 42Mrad/sec$
 - [2] List all possible gains, if different switch settings are used.
 $f = \frac{1}{6}, \frac{2}{6}, \frac{3}{6}, \frac{4}{6}, \frac{5}{6}, 1$ $A_{cl} = 6, 3, 2, 1.5, 1.2, 1$
 - [2] What op-amp topologies would work for this circuit? (list all viable combinations of simple single stage, two stage, FC, FC two stage, and NMOS or PMOS input)
 PMOS input FC 2 stage



5. [11] For the amplifier in the figure to the right
 a. [2] Draw the small signal model labeling the small signal variables v_i , v_o , i_o , v_s



- b. [1] Write an expression for G_m as the ratio of two small signal parameters while a third is held equal to zero.

$$G_m = \frac{i_o}{v_i} \Big|_{v_o=0}$$

- c. [1] Given the conditions above for the calculation of G_m , write v_s in terms of i_o

$$v_s = i_o R_S$$

- d. [2] Given the conditions above for the calculation of G_m , write KCL @ v_o and solve for G_m .

$$\begin{aligned} i_o &= g_m v_s + \frac{1}{r_o} (v_o - v_s) \\ &= g_m v_i + \left(g_m + \frac{1}{r_o}\right) (-v_s) \end{aligned}$$

$$G_m = \frac{i_o}{v_i} = \frac{g_m}{1 + \left(g_m + \frac{1}{r_o}\right) R_S}$$

$$i_o \left[1 + \left(g_m + \frac{1}{r_o}\right) R_S \right] = g_m v_i$$

- e. [3] Find the approximate value for G_m for each of three different values of R_S : much less than $1/g_m$, equal to $1/g_m$, and much greater than $1/g_m$.

$$G_m = \begin{cases} g_m & R_S \ll \frac{1}{g_m} \\ g_m/2 & R_S = \frac{1}{g_m} \\ 1/R_S & R_S \gg \frac{1}{g_m} \end{cases}$$

- f. [1] Write the full expression for R_o . (you don't need to derive it)

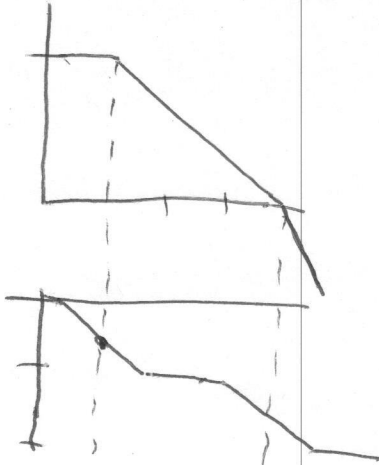
$$R_o = R_D \parallel \left(r_o (1 + g_m R_S) + R_S \right)$$

- g. [1] If R_S is much greater than $1/g_m$, and $R_D = 2R_S$, roughly what is the gain?

-2

6. [13] You have designed a two stage Miller-compensated op-amp with a phase margin of 45 degrees in unity gain feedback. The load capacitance is more than 10 times bigger than any other capacitor in the circuit. You have removed the RHP zero from the compensation capacitor.

a. [5] Carefully sketch a Bode plot of the open-loop gain. Assume that the DC gain is roughly 1000.



b. [2] If you increase the load capacitance by a factor of 10, what happens to the phase margin? Unity gain frequency?

$$PM \approx 0$$

unity gain decreases by $\sqrt{10}$

c. [2] If instead you increase the compensation capacitor by 10x, what happens to the phase margin and unity gain frequency?

$$PM \approx 90$$

ω_u decreases by 10

d. [2] If you increase both the load capacitance and the compensation capacitor by 10x, what happens to the phase margin and unity gain frequency?

both stay the same

e. [2] If you have a single-stage folded cascode op-amp with a unity-gain phase margin of 45 degrees and you increase the load capacitance by 10x, what happens to the phase margin and unity gain frequency?

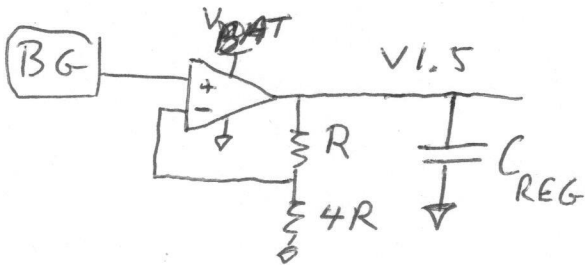
$$PM \approx 90$$

ω_u decreases by 10

7. [12] In your project, you are having some trouble with leakage on the ADC V_{ref} LD switch. You decide that the best solution is to generate another regulated voltage, this one at 1.5V, to use for the gate and body of that PMOS switch.

- [4] Using your bandgap reference of 1.2V, sketch the complete regulator circuit. Start at a high level, with an op-amp symbol, some resistors, etc.
- [4] Show the schematic for your op-amp, including what overdrive voltages you would pick. You may assume that op-amp internal bias voltages are generated elsewhere.
- [2] Discuss the stability of the loop, and how you would guarantee it.
- [2] Also show the circuit that you would use to convert the original LD signal running off of 1.2 V to the new LD_{1.5} signal at 1.5V.

a)



b) Use 2 stage nmos input FC. 2nd stage would have $V_{ov} = 100\mu V$
So would first stage.

Need input compare near top rail, output swing near top rail (100mV)

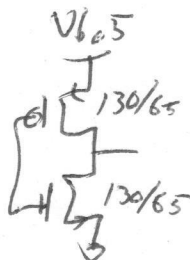
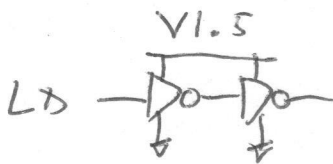
c) need to add a compensation capacitor, for Miller comp.

Size C_{REG} to get low ripple on inverter switching. Probably very small.

So 2nd stage will have high freq. pole. Won't need to compensate much.

Minimum sized devices will be fine, gain fairly low.

d)



9. [12] In the following 2 bit ADC circuit, LD and CMP are non-overlapping clocks. Assume that the RC time constants are fast compared to the time scale below.
- a. [10] Assuming $V_{in}=0.2V$, **carefully sketch** the waveforms on V_x and LOW on the graph provided below. $V_{ref}=1V$. b_1 and b_0 are either 0 or 1V.
- b. [1] What binary value should the SAR report when $V_{in}=0.2$?

00

- c. [1] If the comparator is implemented as an op-amp running from a supply voltage of V_{ref} , what topologies can be used?

NMOS input FC

