



University of California
 College of Engineering
 Department of Electrical Engineering
 and Computer Sciences

E. Alon

Thursday, October 7, 2010
 6:30-8:00pm

EECS 141: FALL 2010—MIDTERM 1

For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

NMOS:

$$V_{Tn} = 0.2V, \mu_n = 400 \text{ cm}^2/(V \cdot s), C_{ox} = 1.125 \text{ } \mu\text{F}/\text{cm}^2, v_{sat} = 1e7 \text{ cm/s}, \lambda = 0$$

PMOS:

$$|V_{Tp}| = 0.2V, \mu_p = 200 \text{ cm}^2/(V \cdot s), C_{ox} = 1.125 \text{ } \mu\text{F}/\text{cm}^2, v_{sat} = 1e7 \text{ cm/s}, \lambda = 0$$

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GRAD/UNDERGRAD	
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Problem 1: ____ / 22

Problem 2: ____ / 22

Problem 3: ____ / 22

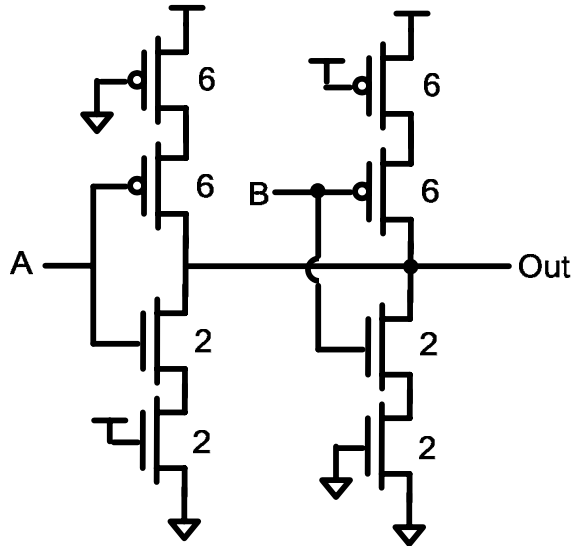
Total: ____ / 66

PROBLEM 1. (22 pts) Complex Gates and Delay.

a) **(6 pts)** Implement the function $F = \overline{((A+B) \cdot C + D)} \cdot E$ with a complex static CMOS gate.

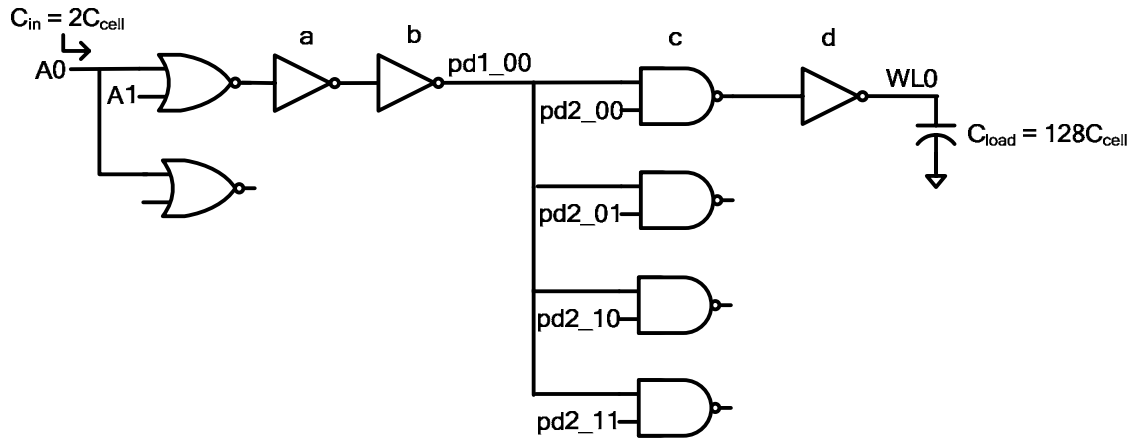
b) **(6 pts)** Assuming $R_{sqp} = 0.5 \cdot R_{sqn}$, size your gate so that the worst-case pull up resistance is equal to the worst-case pull-down resistance. What is the logical effort of this gate from the E input?

- c) (10 pts) Using the switch model for the transistors, what is the delay of the gate shown below when $B = 0V$ and A rises from 0 to V_{DD} ? You can assume that $C_G = C_D = 1.5fF/\mu m$, $R_{sqn} = 10k\Omega/\square$, and $R_{sqp} = 30k\Omega/\square$, and you should provide your answer in ps.



PROBLEM 2. Decoders and Logical Effort (22 points)

Shown below is the critical path of a decoder for a 16x128 SRAM array. This decoder has been implemented by a 2-4 predecoder followed by a 4-16 final decoder.



- a) (6 pts) What is the path effort from A0 to WL0?

- b) (2 pts) What EF/stage minimizes the delay of this decoder?

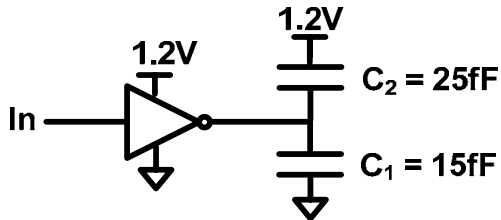
- c) (6 pts) Size the gates to minimize the delay from A0 to WL0.

Size	Value (C_{cell})
a	
b	
c	
d	

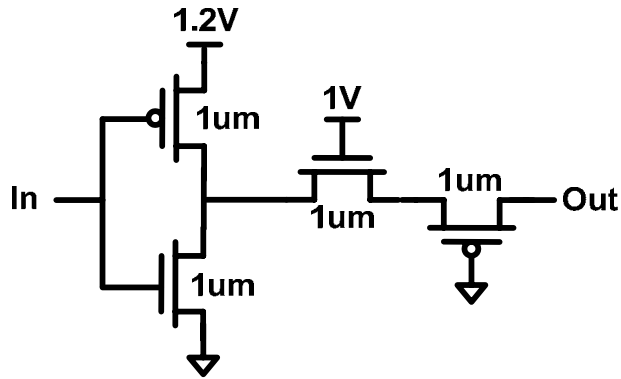
- d) **(8 pts)** Now design a decoder that is optimized for a 16x16 SRAM array. You can use whatever gates you'd like to, but your input capacitance should still be $2 \cdot C_{\text{cell}}$, and you should choose the types and number of gates in order to minimize the total delay. You don't need to draw the entire decoder or size the gates – you just need to draw the critical path (like what we've drawn in part a). However, you should explain why you made the choices you did for this design.

PROBLEM 3. (22 pts) Miscellaneous

- a) **(6 points)** How much energy is pulled out of the 1.2V power supply in the circuit shown below when In steps from 1.2V to 0V? How about when In steps from 0V to 1.2V? You can ignore all capacitors associated with the transistors inside of the inverter.



- b) (8 pts) Using the simple switch model of the transistors with $R_{sqn} = 10k\Omega/\square$, $R_{sqp} = 20k\Omega/\square$, and $V_{TN} = |V_{TP}| = 0.3V$, draw the VTC of the circuit shown below. If the circuit is digital, provide the values of V_{OH} , V_{OL} , V_{IH} , and V_{IL} ; if the circuit is not digital, explain why it isn't digital.



- c) (8 pts) Shown below is a circuit that your colleague claims can be used to implement a digital gate. Using the velocity saturated model, calculate what V_{out} is for all 4 states of the input signals (i.e. $A=B=0$; $A=1, B=0$; $A=0, B=1$; $A=B=1$). What is the logic function implemented by this gate?

