University of California at Berkeley
Department of Electrical Engineering and Computer Science

EECS 141: Final Exam, Fall '96

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Please PRINT your name on each sheet. Write clearly.

Use the space provided to answer all questions. Use the back side if needed.

Name: _____
(last) (first)

SID: _____ Signature: _____

Transistor parameters:

	NMOS	PMOS
V_{T0}	0.7	-1.0
k'_n, k'_p	60 μA/V^2	30 μA/V^2
L_d	0 μm	0 μm

Neglect body effect and
channel-length modulation.

Grades

Problem #1 (18 points)	
Problem #2 (16 points)	
Problem #3 (18 points)	
Problem #4 (16 points)	
Problem #5 (12 points)	
Problem #6 (10 points)	
Problem #7 (12 points)	
Problem #8 (18 points)	
Total (120 points)	

Name:

Problem 1. For each of the following statements, indicate where it is true or false. (18 points)

(T / F) 1(a) The speed of a ring oscillator can continuously be improved by increasing the W/L ratio of the inverters.

(T / F) 1(b) Decreasing supply voltage helps to alleviate the velocity-saturation problem.

(T / F) 1(c) The load capacitance of a static CMOS gate has no effect on its VTC.

(T / F) 1(d) A ϕn-block dynamic gate will not have any charge sharing problems if only $0 \rightarrow 1$ transitions occur at its inputs during evaluation.

(T / F) 1(e) The transistors in a Manchester carry chain should be sized progressively larger from the input to output to reduce the propagation delay.

(T / F) 1(f) Low-swing buses save power and reduce propagation delay at the same time.

(T / F) 1(g) The delay of a static inverter is minimized if $(W/L)_p/(W/L)_n$ is equal to μ_n/μ_p.

(T / F) 1(h) Silicided poly lines reduce the delay of a wire by decreasing the capacitance.

(T / F) 1(i) The maximum propagation delay between two latches determines if a race condition will occur due to clock skew.

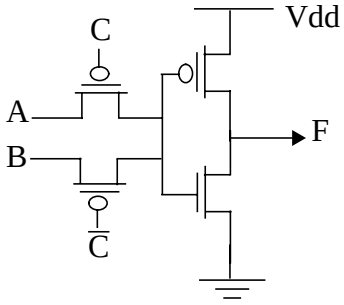
(T / F) 1(j) A 3-transistor DRAM cell requires a sense amplifier to be functional.

(T / F) 1(k) A NAND-based ROM structure is typically more compact and faster than a NOR-based one.

(T / F) 1(l) The number of transistors in a tree column decoder increases linearly with the size of the address word.

Name:

Problem 2. Consider the pass transistor based circuit that Dilbert is using in a low-power application. (16 points)



2(a) Notice that PMOS pass transistors are used instead of NMOS. How does this affect the performance of the circuit? (2 points)

2(b) What is the logic function at the output F? (4 points)

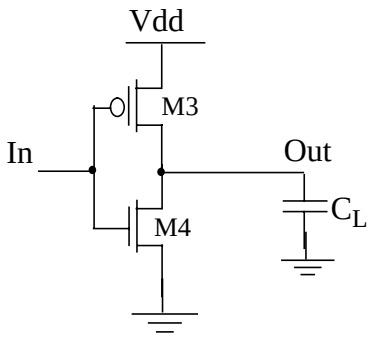
F:

2(c) To eliminate the static power dissipation, Dilbert decides to decrease the 0-level voltage at node C and $\overline{C}$ to below ground. What is the minimum decrease in voltage required to eliminate static power dissipation. (6 points)

2(d) Dilbert is told by his manager that he can't use any negative voltages. Suggest two simple modifications that would eliminate the static power dissipation problem. (4 points)

Name:

Problem 3. The inverter below is driving a 50fF load. Consider the case when the load capacitance is charging from 0 to Vdd. (18 points)



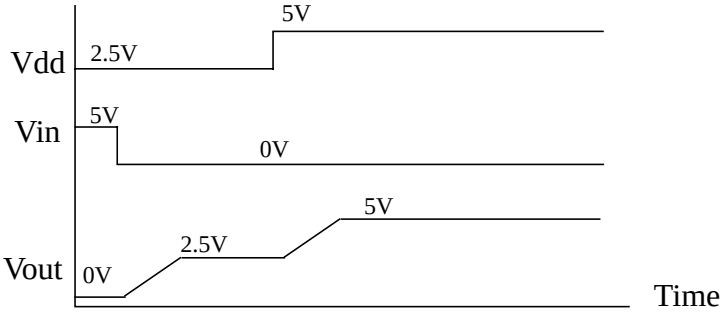
3(a) Vdd = 5V. What is the energy stored in C_L after it is fully charged? (2 points)

Energy:

3(b) Vdd = 5V. What is the energy dissipated in the PMOS? (2 points)

Energy:

Now assume that the supply voltage is not constant but is first held at 2.5V and then changed to 5V as shown below. The output capacitor therefore charges in two phases — from 0 to 2.5V and then from 2.5V to 5V.



Name:

3(c) What is the total energy stored in C_L after it is charged to 5V. (4 points)

Energy:

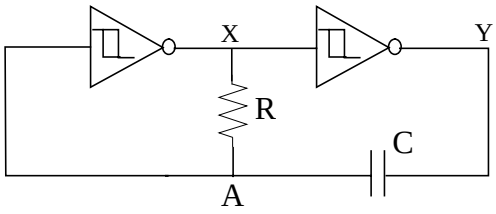
3(d) What is the total energy that is dissipated in the PMOS during the two phases. (6 points)

Energy:

3(e) Suggest one advantage and one disadvantage of this scheme. (4 points)

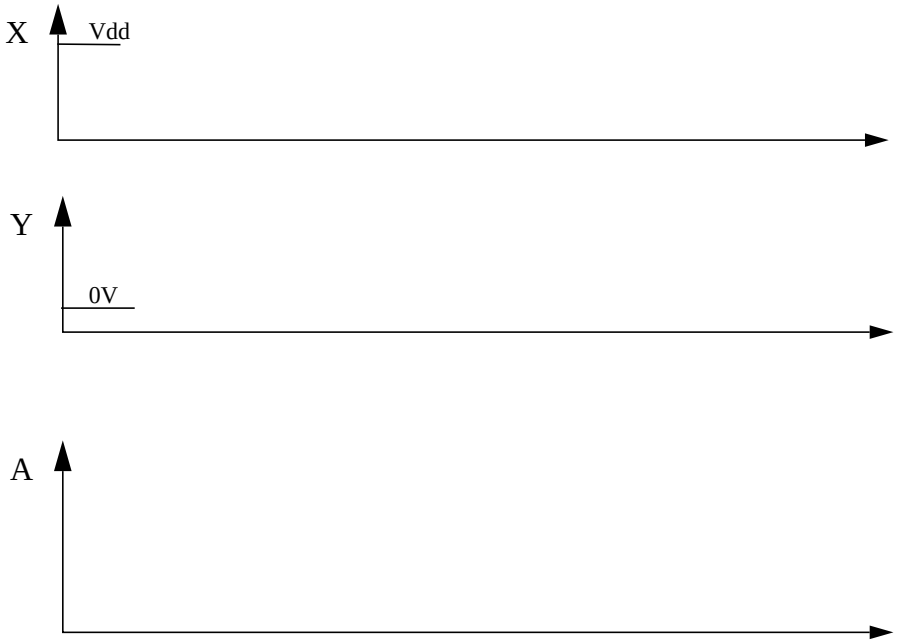
Name:

Problem 4. The circuit below operates at a supply voltage of 3V and uses 2 Schmitt triggers with the following threshold voltages: V_{M+} = 2V, V_{M-} = 1V. (16 points)



4(a) Identify whether the circuit below is monostable, bistable or astable. (2 points)

4(b) Draw the waveforms at node X, Y, and A. Mark all important voltage levels. (6 points)



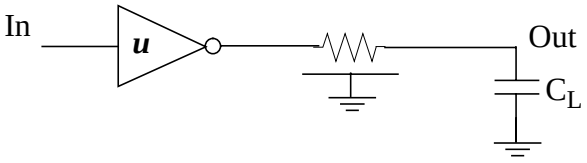
Name:

4(c) Calculate the most important timing parameter for this circuit (propagation delay for bistable, pulse width for monostable, and time period for astable) in terms of R and C. You can assume that gate delays are negligible compared to the delay of the RC network. (8 points)

Time:

Name:

Problem 5. James is required to drive a ***u*** mm long polysilicon wire with a 1pF load at its end (as shown below) using an inverter which is ***u*** times a minimum sized inverter. The poly wire has a capacitance of ***c*** per mm and a resistance of ***r*** per mm. A minimum sized inverter has an input capacitance = C_i and a propagation delay of ***tp0*** when driving an identical inverter. (12 points)



5(a) What is the propagation delay, t_p, of the above circuit in terms the variables given? (6 points)

t_p:

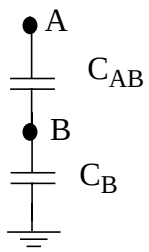
5(b) What value of ***u*** minimizes t_p. (6 points)

u:

Name:

Problem 6.

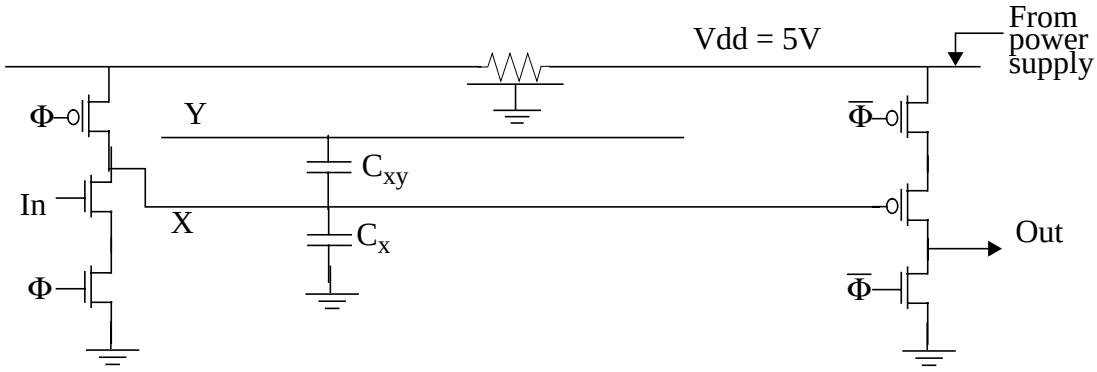
6(a) 2 nodes, A and B, are capacitively coupled to each other and to ground as shown below. Initially, the voltage at A is V_A and that at B is V_B. If the voltage at A drops to 0 volts what is the voltage change on B. (2 points)



ΔV_B:

6(b) The figure below shows two dynamic gates placed far apart. Node X is capacitively coupled with another wire Y which runs parallel to it and can make 0→1 or 1→0 transitions at any time. C_X = 100fF, C_{XY} = 20 fF.

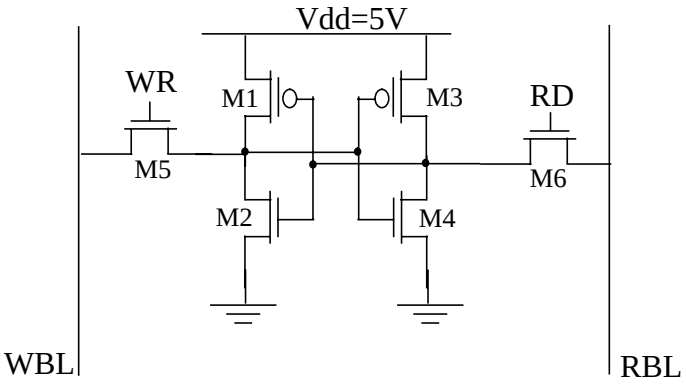
Assume that the supply line behaves as a distributed rc line with r = 0.1 ohm/μm and c = 0.05 fF/μm. Vdd = 5V and the maximum, average and minimum current through the supply line is 1.85mA, 1mA, and 0.15mA, respectively. What is the maximum distance that can be allowed between the two gates without any malfunction. (8 points)



L:

Name:

Problem 7. The figure below shows a SRAM cell that uses separate bit lines for read and write operations. During the write operation WR=Vdd, RD=0V, and during the read operation WR=0V, RD=Vdd. The RBL contains the last voltage read out (i.e. RBL is not precharged to any value). For the inverters, V_M=Vdd/2. Vdd = 5V. Answer the following questions in terms of the (W/L) ratios of M1, M2, M3, and M4. (12 points)



7(a) What is the minimum and maximum voltages that RBL can swing? (2 points)

V_{max}:

V_{min}:

7(b) What is the constraint on $(W/L)_5$ for the memory cell to be functional? (5 points)

$(W/L)_5$:

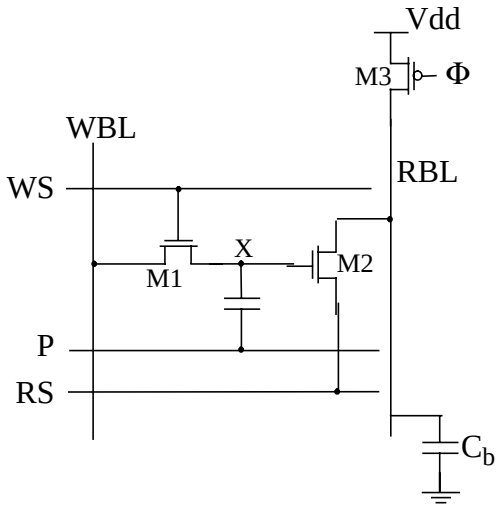
Name:

7(c) What is the constraint on $(W/L)_6$ for the memory cell to be functional? (5 points)

$(W/L)_6$:

Name:

Problem 8. The figure below shows a 2T-DRAM cell to be used in a low-voltage application. The supply voltage is fixed at 1.0V. WBL is the write bit-line, RBL the read bit-line, WL the word-line. Assume initially that node P is fixed at GND. (18 points)

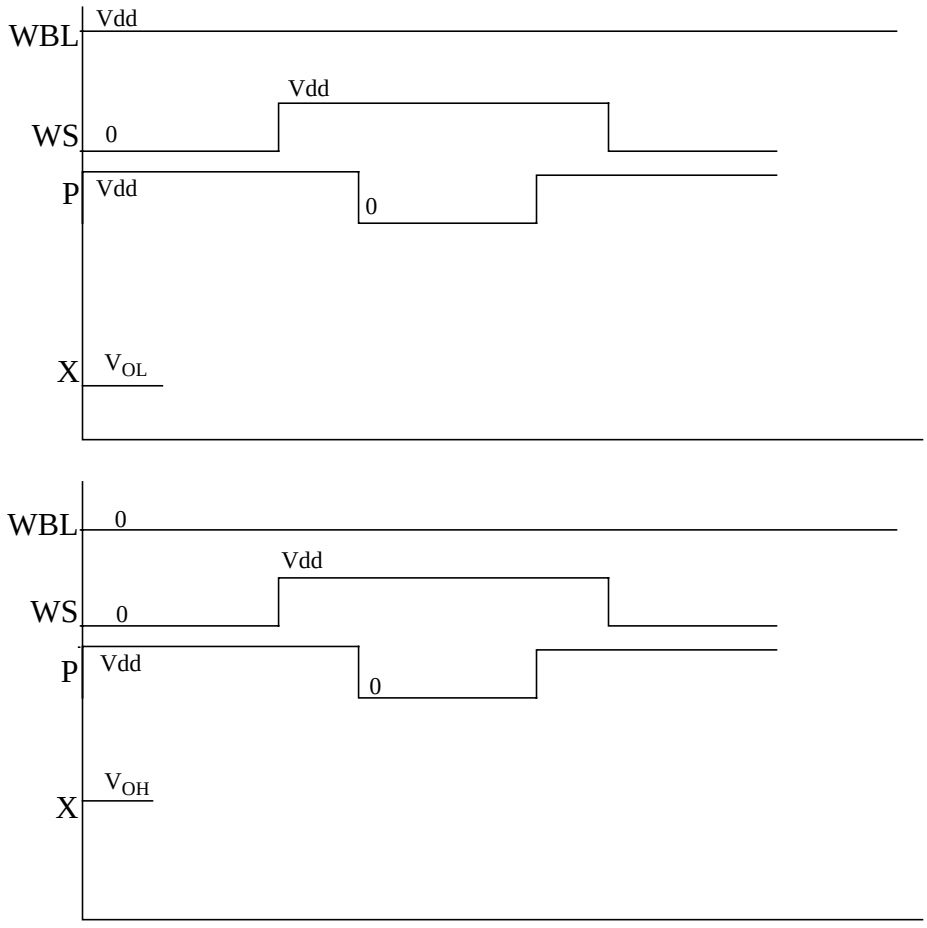


8(a) What are the voltages (Vdd or GND) required on the control signals (WS, RS) to read from this cell. (2 points)

8(b) Will this circuit function correctly? Explain your answer. (4 points)

8(c) Instead of node P being fixed at GND, it has waveform shown below. Fill in the timing diagrams for the write operation. Denote the voltage levels in terms of V_{dd} and V_T. Assume there is enough time to let the transient effects settle out. (8 points)

Name:



8(d) Is the read cycle destructive? Explain your answer. (2 points)

8(e) Does the memory cell require refresh? Why or why not? (2 points)