University of California
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EECS 141: SPRING 04—MIDTERM 1

NAME	Last First

SID	

Problem 1 (on 11):
Problem 2 (on 12):
Problem 3 (on 9):

Total	

PROBLEM 1: MOSFET Devices (11 points)

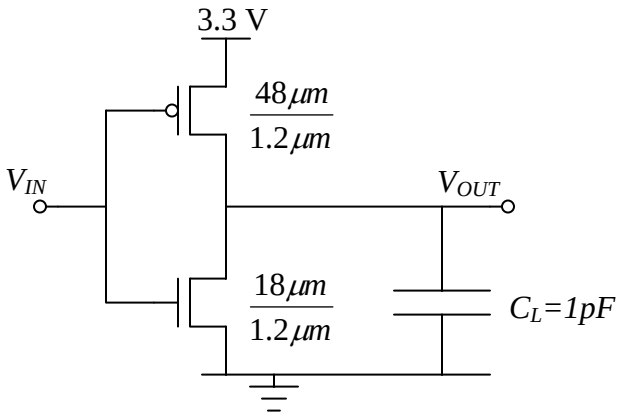
Two MOSFETs fabricated in a long channel process are tested to determine their I/V characteristics. Both devices have W/L = 2.4μm/1.2μm. Measured drain currents for different values of VGS and VDS are as follows (VSB = 0 in all cases):

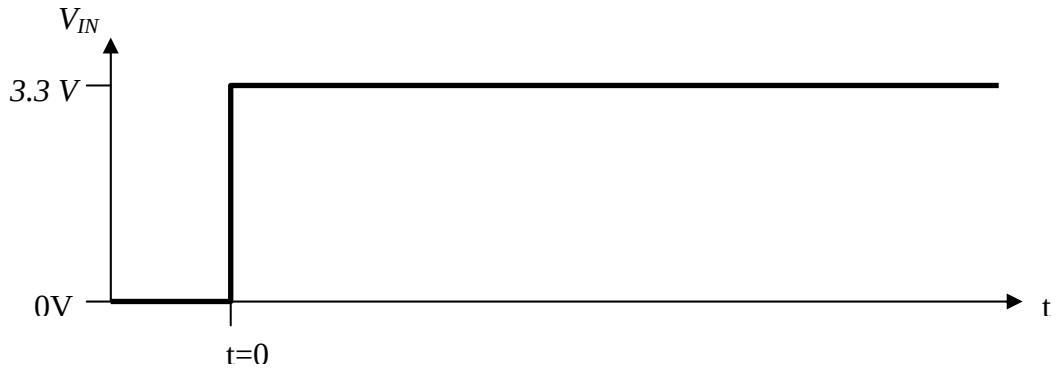
Condition:	**$\|I_D\|$ - MOSFET A**	$\|I_D\|$ - **MOSFET B**
VGS = 0V, VDS = 0V	0A	0A
VGS = -1V, VDS = -2V	20μA	0A
VGS = 1V, VDS = 1V	0A	45μA
VGS = 1V, VDS = 0.02V	0A	4μA
VGS = -2V, VDS = -2V	200μA	0A

a. **(6 points)** Determine the device parameters to complete the following table. Assume λ=0 for both devices.

Parameter:	**MOSFET A**	**MOSFET B**
NMOS or PMOS?		
VT0		
k'		

b. **(5 points)** This fabrication process is now used to make the inverter shown below. On the following graph, sketch the approximate response at V_{OUT} for a rising input step until the transient settles. You may neglect the intrinsic transistor capacitances.
Indicate the region of operation of the two transistors as the transient progresses. **Determine precisely the times at which any changes in region of operation occur**, **and indicate those times on the chart.**




V_{IN}
3.3 V
0V
t
t=0


V_{OUT}
0V
t
t=0

Problem 2: Propagation delay and energy consumption (12 points)

Consider the following circuit. Both PMOS transistor M_1 and NMOS transistor M_2 have the same size with W=0.36μm and L=0.24μm. C_{L1} = C_{L2} =10pF. V_{DD} = 2.5V. Use the transistor parameters, defined in Table 3.2 of the textbook. However, you may assume that **both the body-effect coefficient γ and the channel length modulation factor λ equal 0**.

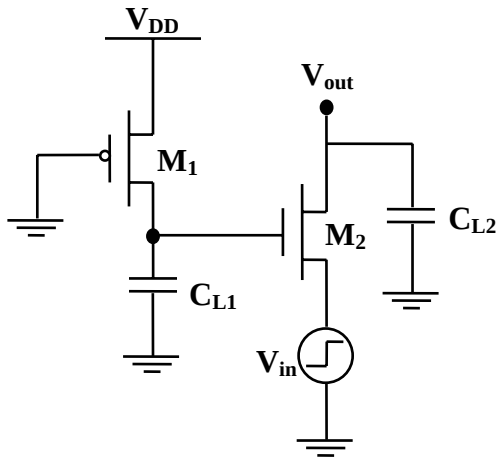


Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

a. **(2 points)** Assume that Vout is initially at 0. V_{in} now experiences a sharp rise from 0 to V_{DD}. Determine the final voltage at V_{out} after all transients have settled.

$V_{out}(t=\infty)$ =

b. **(2 points)** Determine the propagation delay when V_{in} makes a low-to-high transition as described in part a. You can neglect the transistor capacitances of M_1 and M_2 because the load capacitances C_{L1} and C_{L2} are orders of magnitude larger.

$t_p =$

c. **(2 points)** Determine the propagation delay when Vin transitions from Vdd to 0. Assume the same assumptions as in part b.

$t_p =$

d. **(4 points)** Determine E_{LH} (the energy dissipated in the transistors when V_{in} makes a low-to-high transition) and E_{HL} (the energy dissipated in the transistors when V_{in} makes a high-to-low transition).

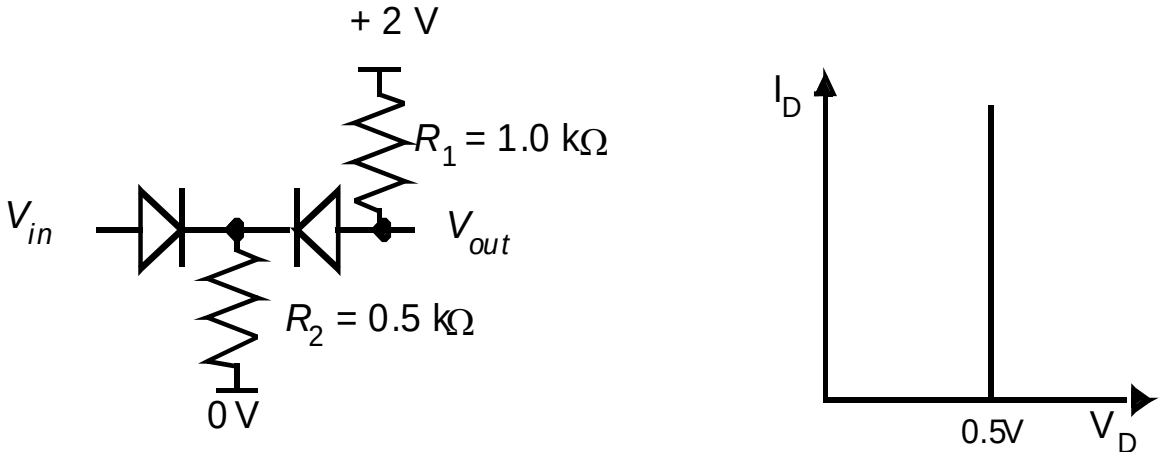
$E_{LH} =$

$E_{HL} =$

e. **(2 points)** In one sentence explain how you would reduce the propagation delay from V_{in} to V_{out}. Is there a limit using this method? If the answer is yes, give the lower limit of the propagation delay using only a few words. No calculation is needed.

Problem 3: Voltage Transfer Characteristic (9 points)

Consider the diode circuit shown below. The I-V characteristic of the diodes is given by the chart on the right side.



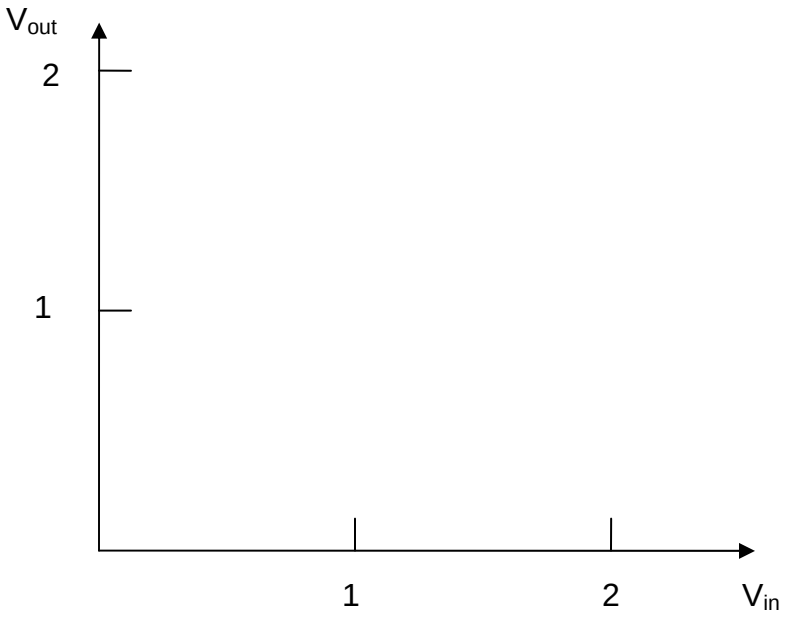
a. **(2 point)** Determine the value of Vout for Vin = 0V.

V_{out} (V_{in} = 0V) =

b. **(2 point)** What is the value of Vout when Vin = 2V.

V_{out} (V_{in} = 2V) =

c. **(2 points)** Draw the complete voltage transfer characteristic of the gate (for V_{in} going from 0 to 2V).



d. **(1 points)** Revisit question (a), assuming now that the gate has a fanout of one identical gate.

V_{out} (V_{in} = 0V) =

e. **(2 points)** Revisit question (b), assuming that the gate has a fanout of one identical gate.

V_{out} (V_{in} = 2V) =