

Problem 1: Logic Design

a. Derive a **static NMOS pass-transistor** implementation of the following logic function: $F = \overline{(a+b).c}$, so that the number of transistors is minimized. The implementation should include a static inverter at the output. You may assume that the complements of a , b , and c are available.

b. Discuss the **sizing of the transistors in the pass-transistor network**, assuming that maximum performance is the intended goal.

- Explain briefly qualitatively why increasing the transistors indiscriminately does not necessarily lead to an improvement in performance.

- Explain the method you would use to choose the transistor sizes (assume here that all the transistors in the pass-transistor network are of an identical size). Draw the equivalent circuit that you would use and its components.

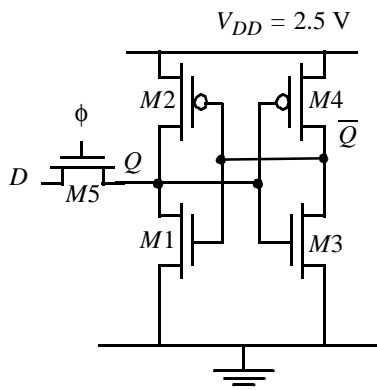
• Would you keep all the transistors in the pass-transistor network identical? If not, which transistors would you make larger (Name the transistors on the schematic M1, M2, etc ...)?

c. The switching threshold of the output inverter can be modified by changing the ratio of PMOS and NMOS devices. Which option is preferable from a performance perspective?

- Keep the switching threshold in the middle.
- Move switching threshold up.
- Move the switching threshold down.

Explain your answer.

PROBLEM 2: Flip-Flop



$$M1 = M3 = 1.8\mu\text{m}/1.2\mu\text{m}$$

$$M2 = M4 = 5.4\mu\text{m}/1.2\mu\text{m}$$

A five-transistor D flip-flop cell is drawn below. Assume that the clock ϕ switches between 0 and 2.5 V.

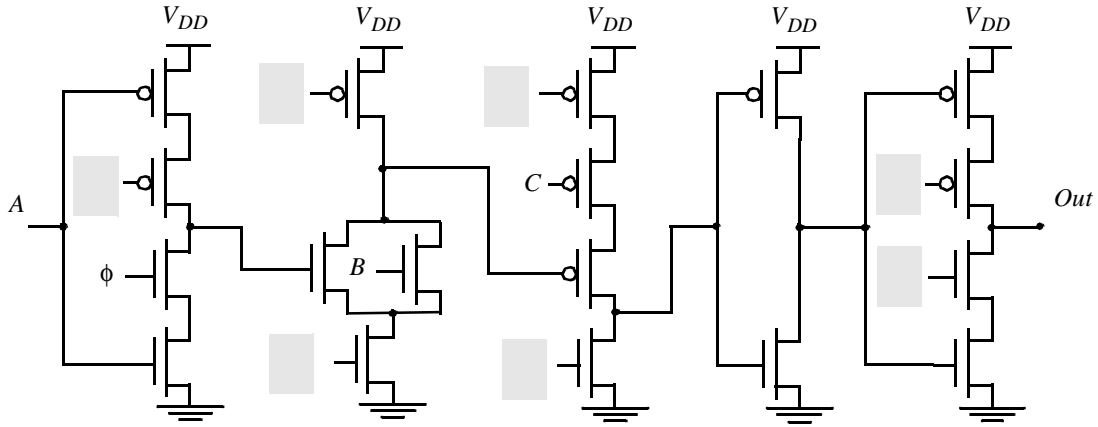
a. Determine the size constraints on transistor M_5 so that a 0 can be written in the cell.

b. Determine the size constraints on transistor M_5 so that a 1 can be written in the cell.

c. Explain qualitatively how you would resize the transistors in the cross-coupled inverter pair to alleviate the worst case condition.

PROBLEM 3: Timing

Consider the following circuit (implemented in the 1.2 μm CMOS technology). Assume $V_{DD} = 3\text{ V}$.



- Fill in the missing clock connections on the schematics (marked by the gray boxes) so that the circuit will operate correctly. For each connection you can choose between ϕ and $\bar{\phi}$ (you may assume here that they are non-overlapping and that there is no skew).
- The circuit **cascades** a number of dynamic and static logic stages. Will the proposed configuration evaluate correctly (assuming no clock overlap and ignoring leakage and clock feedthrough)? **Explain why or why not.**

c. Is the circuit sensitive to clock overlaps between ϕ and $\bar{\phi}$. **Explain your answer.**

d. Is the circuit sensitive to clock skew? Assume for instance that the output latch is located at a very remote site on the chip. **Explain your answer.**

e. Assume that a network is sensitive to clock skew, determine which approaches would help to cure the problem:

- Reduce the clock frequency
- Route the clock in the opposite direction of the data
- Increase the size of the clock driver to create sharper clock edges
- Resize the logic transistors to reduce the minimum logic delay between the latches
- Resize the logic transistors to increase the minimum logic delay between the latches