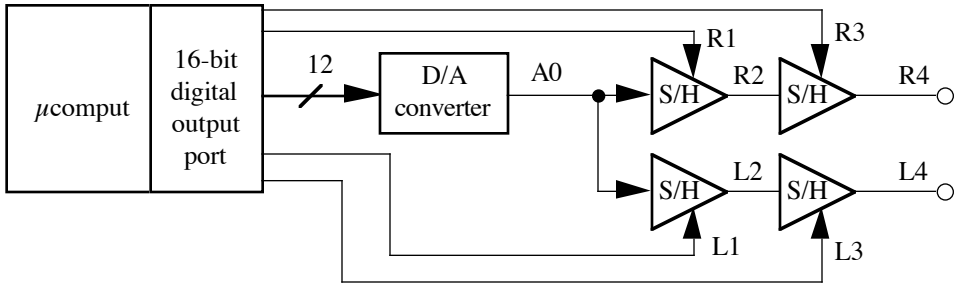
Solutions for Midterm #1 - EECS 145M Spring 2006

1 When the input number changes in more than one bit, it is impossible for both bit switches to change exactly at the same time. During the brief time between the first switch change and the last switch change, an erroneous voltage will be produced.

[4 points off for settling time and no mention of bit changes]

[2 points off for not stating that the bits cannot change simultaneously]

2.1



R1, R3, L1, and L3 are digital control lines to S/H amps

[2 points off for using only two S/H amps, a design that does not update both left and right within << 1 μs]

2.2

1 start loop with i = 1, write HOLD to L3 and R3

2 write left[i] to 12 bits of digital output port, write HOLD to R1, L3 and R3 and write SAMPLE to L1

3 write left[i] to 12 bits of digital output port, write HOLD to L1, R1, L3, and R3

Note: this hold command takes effect 1 μs after the new D/A input – much longer than its 100 ns settling time.

4 write right[i] to 12 bits of digital output port, write HOLD to L1, L3 and R3, and write SAMPLE to R1

5 write right[i] to 12 bits of digital output port, write HOLD to L1, R1, L3, and R3

6 write HOLD to L1 and R1, and write SAMPLE to L3 and R3 (12 bit input to D/A does not matter)

7 write HOLD to L1 and R1, L3 and R3 (12 bit input to D/A does not matter)

8 wait until a total of 25 μs (1000 cycles of the 25 ns clock) have passed in the loop

9 set i = i + 1 and go back to step 2 until all values are exhausted

[3 points for not accounting for all 16 bits during the first four write operatons.]

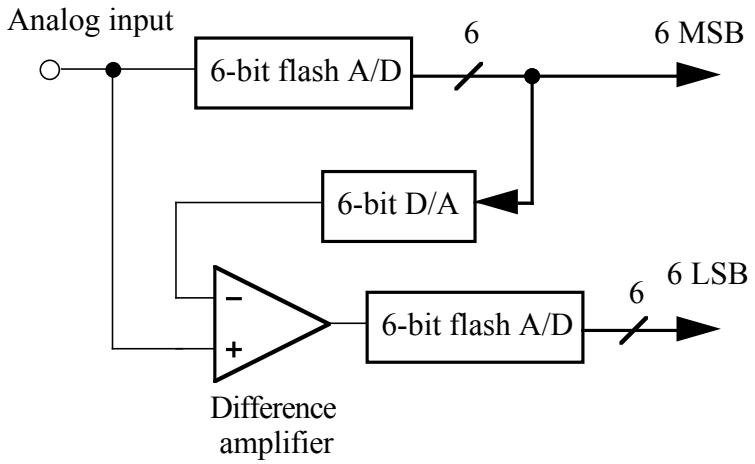
[3 points off if not 40 kHz] [3 points off if left and right updates not simultaneous]

[3 points off if analog outputs not glitch free]

2.2 (3600 s/hr) x (2 hr) x (2 bytes per word) x (2 channels) x(40,000 Hz) = 1152 Mbytes = 9.216 Gbits of storage.

6.912 Gbits was also accepted, assuming efficient packing of 12 bit data

3.1



S/H amplifier or holding capacitors were not required for full credit

[2 points off if difference between D/A output and input was not generated]

3.2

1 Use one 6-bit flash A/D converter to determine the 6 most significant bits

2 Use the 6-bit D/A converter to convert the 6 most significant bits into an analog voltage

3 Use a difference amplifier to subtract the 6-bit D/A output from the analog input

4 Use the second 6-bit flash A/D converter to convert the analog difference from step 3 into the 6 least significant bits

3.3 An N-bit flash converter has 2^N resistors in its resistor ladder. So a 6-bit flash converter has $2^6 = 64$ resistors

[2 points off for 6 or 12] [1 point off for 32] [3 points off for 2^{12}]

3.4 An N-bit R-2R D/A converter has 2N resistors in its resistor ladder. So a 6-bit R-2R D/A converter has 2N = 12 resistors plus one or two additional.

[1 point off for 6; two points off for 3, 4, or 64]

3.5 The 6-bit A/D converter that determines the 6 most significant bits and the 6-bit D/A converter that converts these into an analog voltage must be so accurate that the output of the difference amplifier is accurate to 1/8 step size out of $2^{12} = 4096$ steps or one part in 32k. Since their accuracy is determined by the accuracy of their resistors, a resistor accuracy of 1 part in 32k would be safe.

Here is an example: Imagine that the first stage has 64 steps each 64 mV wide for a total of 4096 mV and the second stage has 64 steps each 1 mV wide. Since the entire 12-bit converter has 1 mV steps and an absolute accuracy of 1/8 LSB, the transition voltages of the first stage must be accurate to 1/8 mV. As a worst case, imagine that the first 32 resistors of the first stage have resistance R + e and the second 32 resistors have resistance R – e, where e is a resistance error. The voltage at the center point of the resistor string of the first stage would then be 4096 mV [32 (R + e) / 64R], which would be 2048 mV plus a error of 2048 mV (e/R) < 1/8 mV. This means that e/R < 1/16,000 and the resistors must be accurate to 1 part in 16k. Note that statistical analysis does not apply if the errors are systematic.

The 6-bit A/D converter that determines the 6 least significant bits only needs to have the accuracy of a 6-bit converter, so the resistors need an accuracy of one part in 2^9, or one part in 512.

[Full credit for resistor accuracy 1 part in 32k or 1 part in 16k]

[4 points off for 1/8 LSB] [3 points off for 1 part in 512]

[asking for a resistor accuracy of "1/8 LSB" will not be meaningful to a resistor manufacturer]

EECS145M Midterm #1 class statistics:

Problem	max	average	rms
1	10	9.8	0.6
2	45	41.2	2.5
3	45	42.8	2.4
total	100	93.8	3.9

Grade distribution:

Range	number	*approximate* letter grade
75-79		
80-84		
85-89	2	B
90-94	5	B+
95-99	4	A
100	1	A+