UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

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	Thursday, March 8, 2012	**SPRING 2012**

You should write your results on the exam sheets only. Partial credit will be given only if you show your work and reasoning clearly.

Throughout the exam, you can ignore flicker noise, assume that the r_o of the transistors is infinite, and ignore all capacitors except those drawn in the circuit unless the problem states otherwise.

Name: Solutions

SID: ______________________

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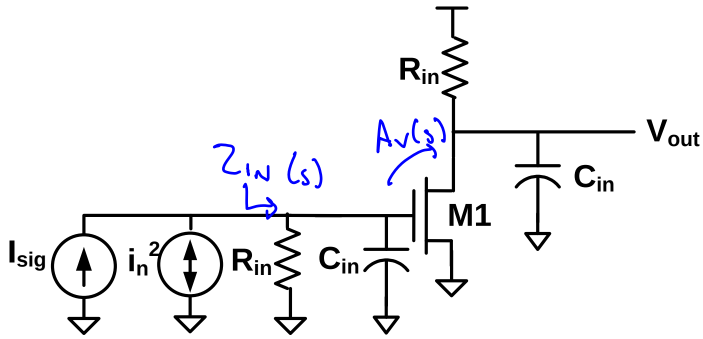
Problem 1 (16 points) Noise and SNR



In this problem we will be examining the circuit shown above, where I_{sig} is a sinusoidal input current with an amplitude of A_I and angular frequency ω, and i_n^2 is a white noise current source with a power spectral density of $4kT/R_n$.

a) **(4 pts)** What is the s-domain transfer function that both I_{sig} and the noise current i_n^2 experience to arrive at V_{out}? You can assume that the transistor M1 is biased in saturation with a given g_m.

$$Z_{in}(s) = \frac{R_{in}}{1+sR_{in}C_{in}} \qquad A_v(s) = \frac{-g_m R_{in}}{1+sR_{in}C_{in}}$$

$$\frac{V_{out}(s)}{I_{in}(s)} = Z_{in}(s) \cdot A_v(s)$$

$$\boxed{\frac{V_{out}(s)}{I_{in}(s)} = \frac{-g_m R_{in} \cdot R_{in}}{(1+sR_{in}C_{in})^2}}$$

b) **(4 pts)** Given your answer to part a), what is the voltage noise variance at V_{out} due to i_n^2 (i.e., $V_{out}^2(i_n)$)? You should provide your answer in terms of R_{in}, C_{in}, g_m, R_n, and kT.

$$V_{out}^2(i_n) = 4kT \cdot \frac{1}{R_N} \cdot \int_0^\infty \left|\left| \frac{V_{out}(f)}{i_N(f)} \right|\right|^2 df$$

* Expand denominator of $\frac{V_{out}(s)}{I_{in}(s)}$ to make integral result more obvious:

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{-g_m R_{IN} \cdot R_{IN}}{s^2 (R_{IN} C_{in})^2 + 2 R_{IN} C_{IN} s + 1}$$

$$\hookrightarrow V_{out}^2(i_N) = 4kT \cdot \frac{1}{R_N} \cdot \frac{(g_M R_{IN})^2 R_{IN}^2}{8 R_{IN} C_{IN}}$$

$$= \boxed{\frac{kT}{C_{IN}} \cdot \frac{R_{IN}}{2R_N} \cdot (g_m R_{IN})^2}$$

c) **(8 pts)** What are the mean-squared signal voltage (i.e., $V_{out}^2(I_{sig})$) and the SNR (i.e., $V_{out}^2(I_{sig})/V_{out}^2(i_n)$) at V_{out}? Note that you can ignore any noise from the transistors/resistors, and that you should provide your answer in terms of ω, A_I, and the same quantities as part b).

$$V_{out}^2(I_{sig}) = \frac{A_I^2}{2} \cdot \left\| \frac{V_{out}(j\omega)}{I_{in}(j\omega)} \right\|^2$$

$$= \boxed{\frac{A_I^2}{2} \cdot \frac{(g_m R_{in})^2 \cdot R_{in}^2}{(1+\omega^2 R_{in}^2 C_{in}^2)^2}}$$

$$SNR = \frac{A_I^2}{2} \cdot \frac{(g_m R_{in})^2 \cdot R_{in}^2}{(1+\omega^2 R_{in}^2 C_{in}^2)^2} \cdot \frac{C_{in}}{kT} \cdot \frac{2R_N}{R_{in}} \cdot \frac{1}{(g_m R_{in})^2}$$

$$= \boxed{\frac{A_I^2 R_N}{kT} \cdot \frac{R_{in} C_{in}}{(1+\omega^2 R_{in}^2 C_{in}^2)^2}}$$

d) **(BONUS)** If we express $R_{in}C_{in}$ as K_{bw}/ω, what choice of K_{bw} would result in the maximum SNR for this circuit?

$$SNR = \frac{A_I^2 R_W}{kT\omega} \cdot \frac{K_{bw}}{(1+K_{BW}^2)^2}$$

$$\frac{\partial SNR}{\partial K_{BW}} = \frac{A_I^2 R_W}{kT\omega} \cdot \frac{(1+K_{BW}^2)^2 - K_{BW} \cdot 2(1+K_{BW}^2) \cdot 2K_{BW}}{(1+K_{BW}^2)^2} = 0$$

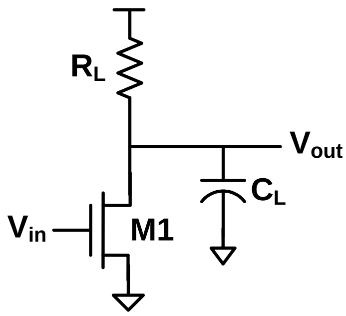
$$1+K_{BW}^2 - 4K_{BW}^2 = 0$$

$$3K_{BW}^2 = 1$$

$$\boxed{K_{BW,opt} = \frac{1}{\sqrt{3}}}$$

Problem 2 (12 points) Amplifier Power

a) **(4 pts)** How much bias current is required for the amplifier shown below to achieve a gain of A_v and bandwidth of ω_{bw}? You should provide your answer in terms of A_v, ω_{bw}, C_L, and the V* of M1.



Gain-bandwidth $= \frac{g_m}{C_L} = A_v w_{BW}$

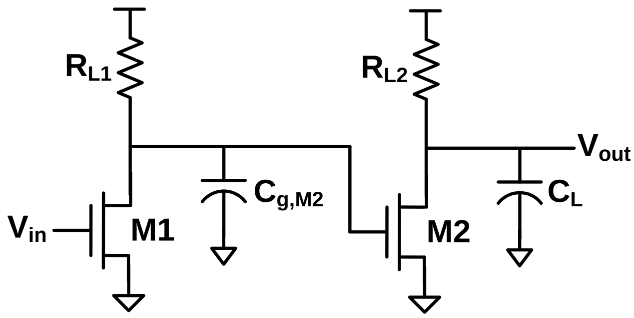
$\hookrightarrow g_m = A_v w_{BW} C_L$

$g_m = \frac{2 I_D}{V^*}$

$\hookrightarrow I_D = \frac{1}{2} g_m V^*$

$$\boxed{I_D = \frac{1}{2} A_v w_{BW} C_L V^*}$$

b) **(8 pts)** Now let's see what happens if we try to achieve the same total gain Av and bandwidth ω_{bw} using the two stage design show below. For simplicity, let's assume that we will make the gains and bandwidths of each individual amplifier stage identical, that the V*'s of M1 and M2 are identical, and that the bandwidth of a circuit with two poles at ω_p is $\omega_p/2$ (i.e., the overall bandwidth of the two stage amplifier is half the bandwidth of each individual stage). Under these conditions, how much total bias current ($I_{M1} + I_{M2}$) is required to achieve the same total gain and bandwidth? You should provide your answer in terms of the ω_T ($=g_m/C_g$) of the transistors and the same parameters as part a).



* To achieve same total gain, $A_{stage}^2 = A_V$

↳ $A_{stage} = \sqrt{A_V}$

* To achieve same total bandwidth, $\omega_{stage}/2 = \omega_{BW}$

↳ $\omega_{stage} = 2\omega_{BW}$

* I_D for 2nd stage: $I_{D2} = \frac{1}{2} \cdot \sqrt{A_V} \cdot 2\omega_{BW} \cdot C_L \cdot V^*$

$I_{D2} = \sqrt{A_V}\, \omega_{BW}\, C_L V^*$

* $g_{m2} = 2\sqrt{A_V}\, \omega_{BW}\, C_L$ $\qquad \frac{g_{m2}}{C_{g2}} = \omega_T$

$C_{g2} = 2\sqrt{A_V}\, \frac{\omega_{BW}}{\omega_T} \cdot C_L$

$I_{D1} = \frac{1}{2}\sqrt{A_V} \cdot 2\omega_{BW} \cdot V^* \cdot \left(2\sqrt{A_V}\, \frac{\omega_{BW}}{\omega_T} \cdot C_L\right)$

↳ $\boxed{I_{D1} + I_{D2} = \sqrt{A_V}\, \omega_{BW}\, C_L V^* \cdot \left(1 + 2\sqrt{A_V}\, \frac{\omega_{BW}}{\omega_T}\right)}$

c) **(BONUS)** Under what condition will the two-stage design from part b) require less bias current then the single stage design from a)?

$$\frac{I_{D1}+I_{D2}}{I_D} < 1 \rightarrow \frac{\sqrt{A_V}\,\omega_{3W}\,C_L V^*\left(1+2\sqrt{A_V}\,\frac{\omega_{3W}}{\omega_T}\right)}{\frac{1}{2}A_V\,\omega_{3W}\,C_L V^*} < 1$$

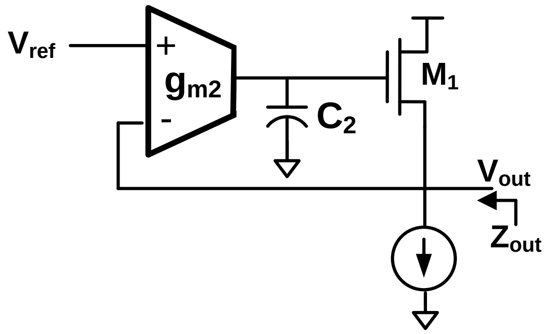
$$\frac{2}{\sqrt{A_V}}\cdot\left(1+2\sqrt{A_V}\,\frac{\omega_{3W}}{\omega_T}\right) < 1$$

$$2\sqrt{A_V}\,\frac{\omega_{3W}}{\omega_T} < \frac{\sqrt{A_V}}{2} - 1$$

$$\boxed{\frac{\omega_{3W}}{\omega_T} < \frac{1}{4} - \frac{1}{2\sqrt{A_V}}}$$

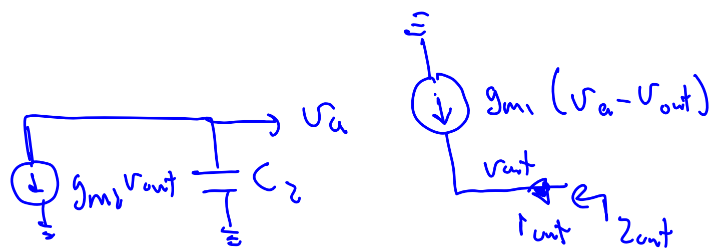
Problem 3 (12 points) Voltage Source Design

In this problem we will examine how to use the structure shown below (which happens to bear some resemblance to a gain-boosted cascode) in order to build a voltage source with a low output impedance. Note that you can assume that the OTA (g_{m2}) is ideal.



a) **(6 pts)** As a function of g_{m1}, g_{m2}, and C_2, what is the s-domain output impedance $Z_{out}(s)$ of the circuit shown above?

Small signal model:



$$i_{out} = g_{m1}(v_{out} - v_a)$$

$$i_{out} = g_{m1}\left(v_{out} - \left(\frac{-g_{m2}}{sC_2}\right)v_{out}\right)$$

$$i_{out} = g_{m1}\left(1 + \frac{g_{m2}}{sC_2}\right)v_{out}$$

$$\frac{v_{out}}{i_{out}} = \frac{1}{g_{m1}(1 + g_{m2}/sC_2)}$$

$$\boxed{Z_{out} = \frac{1}{g_{m1}} \cdot \frac{sC_2/g_{m2}}{sC_2/g_{m2} + 1}}$$

("Easy" way: effective g_{m1} is just $g_{m1}\left(1 + \frac{g_{m2}}{sC_2}\right)$)

b) **(6 pts)** Assuming that g_{m1} = 10mS and that we would like to make sure that at 100MHz the magnitude of the output impedance (i.e., ‖Zout(j*2π*100MHz)‖) is less than 10Ω, what is the minimum gain-bandwidth (i.e., g_{m2}/C_2) required of the OTA in part a)? You should provide your answer in Hz.

* "Easy" (approximate) method:

$\frac{1}{g_{m1}} = 100\Omega$, but target $Z_{out} = 10\Omega$ @ 100MHz

So, OTA needs to provide a gain of ~10 at 100MHz

↳ Gain-Bandwidth = 10 · 100MHz = $\boxed{1\text{GHz}}$

* Precise method:

$$\|Z_{out}\|^2 = \frac{1}{g_{m1}^2} \cdot \frac{w^2 \cdot C_2^2/g_{m2}^2}{w^2 C_2^2/g_{m2}^2 + 1} = Z_{target}^2$$

$$\hookrightarrow w^2/(g_{m2}/C_2)^2 = g_{m1}^2 Z_{target}^2 \left(1 + w^2/(g_{m2}/C_2)^2\right)$$

$$\left(g_m^2 Z_{target}^2 - 1\right) \cdot \frac{w^2}{(g_{m2}/C_2)^2} = -g_m^2 Z_{target}^2$$

$$\frac{w^2}{(g_{m2}/C_2)^2} = \frac{g_m^2 Z_{target}^2}{1 - g_m^2 Z_{target}^2}$$

$$\frac{g_{m2}}{C_2} = \frac{\sqrt{1 - g_m^2 Z_{target}^2}}{g_m Z_{target}} \cdot w$$

$$\frac{g_{m2}}{C_2} = \frac{\sqrt{1 - 0.1^2}}{0.1} \cdot w \rightarrow \boxed{GBW \approx 995\text{MHz}}$$