Electrical Engineering 42/100
Summer 2012
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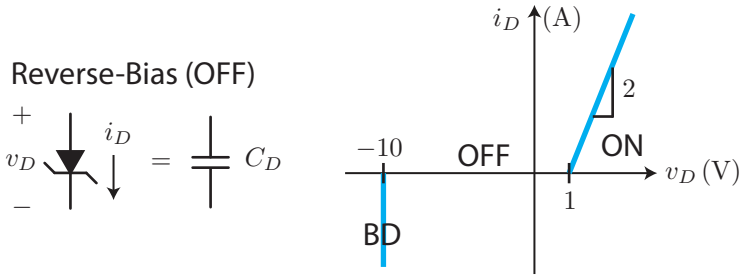
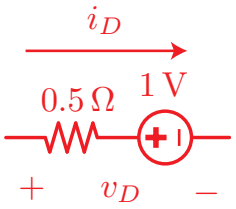
Final Exam Solutions

1. **Diodes Have Capacitance?!?!**

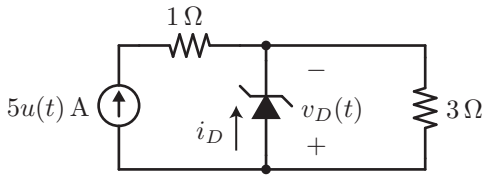
   Frustrated at how inaccurate all our linear diode models have been, John decides to cook up another one. The Zener diode below has a linear ON characteristic and a breakdown voltage V_B like any other, but it is modeled as a *capacitor* C_D when it is reverse-biased, or OFF.



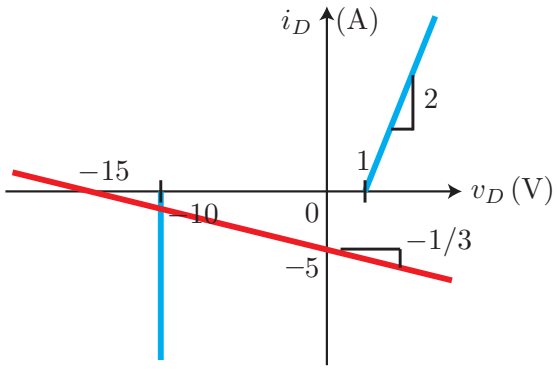
   (a) *(3 points)* Let's first analyze the diode in its forward-bias (ON) mode. What is its linear circuit equivalent in this region of operation? Label the directions of v_D and i_D.

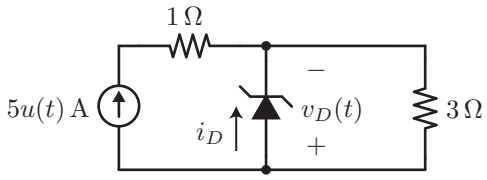


   (b) *(3 points)* John attaches this diode to a circuit as shown below.



   Evidently, the Zener diode is now reverse-biased. On the plot below, draw in the load line immediately after the current source turns on, i.e., $t = 0_+$. Be sure to label slopes and intercepts; your plot need not be to scale.





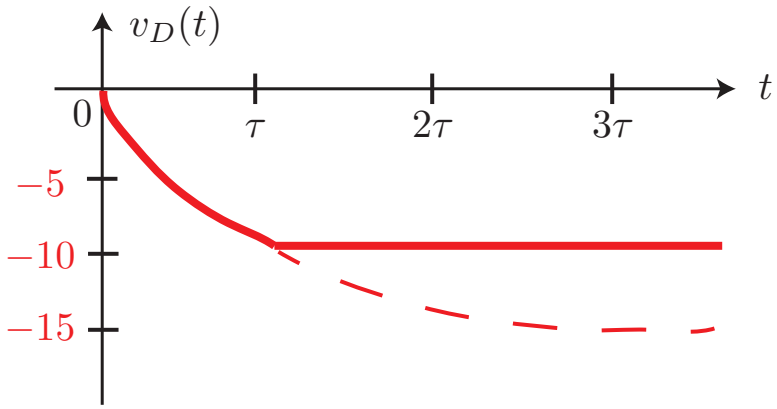
(c) *(3 points)* Suppose the "capacitance" of the diode is $C_D = 1\,\mu\text{F}$ ($10^{-6}\,\text{F}$). What is the time constant τ associated with it?

The time constant is given by $\tau = RC_D$, where R is the Thévenin resistance as seen by the diode/capacitor. Since the current source becomes an open, the $1\,\Omega$ resistor has no effect, and we simply have

$$\tau = RC_D = (3\,\Omega)(1\,\mu\text{F}) = \boxed{3\,\mu\text{s}}$$

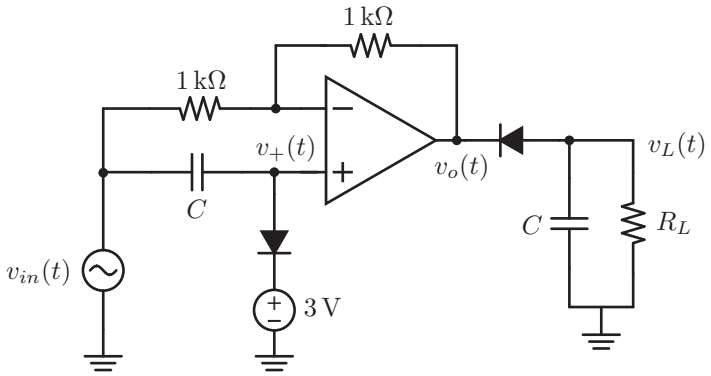
(d) *(6 points)* Sketch the voltage $v_D(t)$ across the diode as a function of time. Label key values on the v_D axis. Remember that a charging capacitor reaches about 63% of its final value after one time constant τ. **Don't forget to account for the diode's breakdown region!**

The "capacitor" naturally wants to exponentially charge up to the steady-state value, which is $-15\,\text{V}$ (obtained if you treat the capacitor as an open circuit). However, this voltage abruptly ends at $-10\,\text{V}$, the breakdown voltage of the diode.



2. **Moar Diode Madness**

William is having so much fun with diodes that he has constructed the following nightmare. Fortunately, you remember that you can always break the problem up into pieces that you can analyze separately.



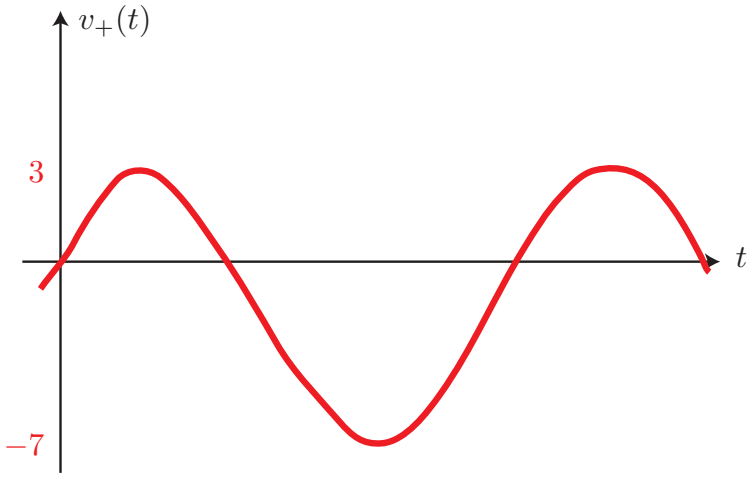
For this entire problem, we can make the following assumptions:

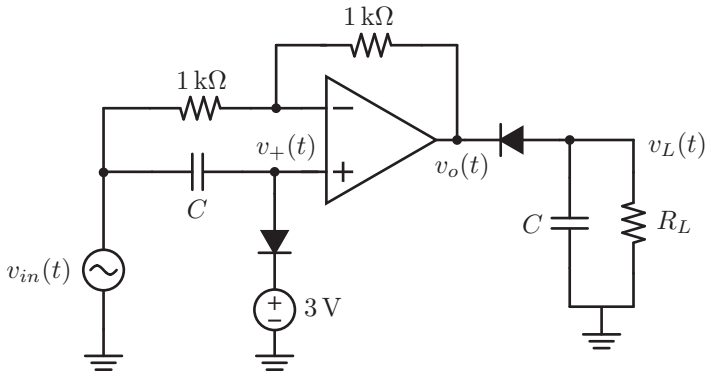
- We are in AC steady-state, such that we can ignore all transient effects.
- The capacitances C are large, such that discharging effects are negligible.
- The op amp is ideal.
- All diodes are ideal with a turn-on voltage of 0 V.

Finally, the input signal is $v_{in}(t) = 5\sin(t)\,\text{V}$.

(a) *(5 points)* Sketch the voltage $v_+(t)$. Be sure to label peak values.

This part of the circuit simply clamps the positive peak of the waveform to 3 V.





(b) *(5 points)* Find an expression for $v_o(t)$ in terms of $v_+(t)$ and $v_{in}(t)$.

Using KCL at the inverting input of the op amp along with SPC ($v_+ = v_-$), we obtain

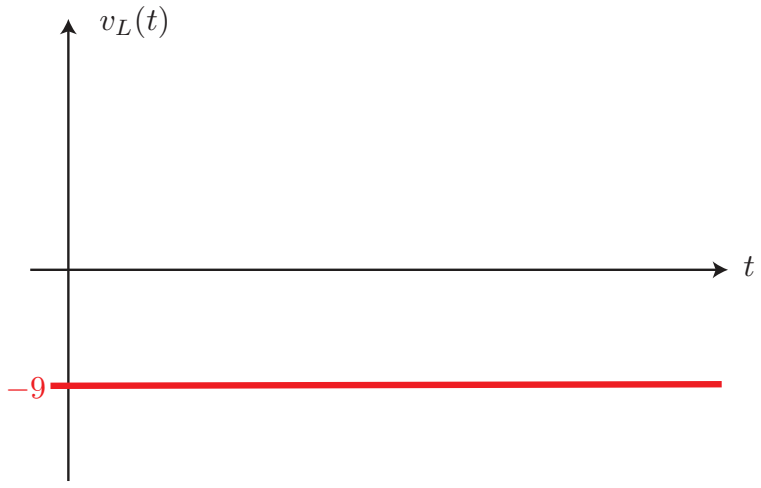
$$\frac{v_+ - v_{in}}{1\,\text{k}\Omega} + \frac{v_+ - v_o}{1\,\text{k}\Omega} = 0$$

$$\boxed{v_o(t) = 2v_+(t) - v_{in}(t)}$$

(c) *(5 points)* We're almost there! Given what you found above, sketch the voltage $v_L(t)$. Be sure to label peak or constant values. **Remember that we don't care about transient effects!**

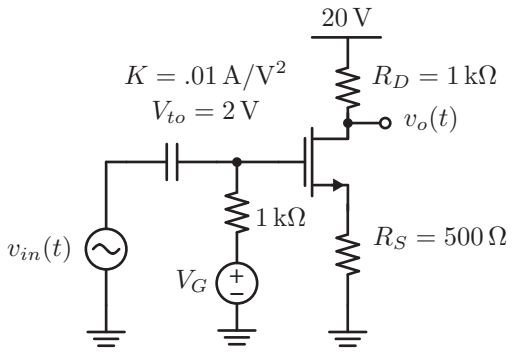
Notice that the output side of the op amp is simply a peak detector with the diode facing backwards. Assuming negligible discharge, $v_L(t)$ will keep constant at the minimum value of $v_o(t)$. According to our expression above, the minimum value is

$$v_L(t) = v_{o,min} = 2v_{+,min} - v_{in,min} = 2(-7) - (-5) = -9\,\text{V}$$



3. **FFFFFFFFUUUUUUUUUU**

Jerry is trying to design an amplifier for the hundredth time. This time, he has turned to MOSFETs, specifically the common-source configuration. He has pulled up the following NMOS specs and designed the circuit as follows.



(a) *(10 points)* Recall that the transconductance of the transistor is given by

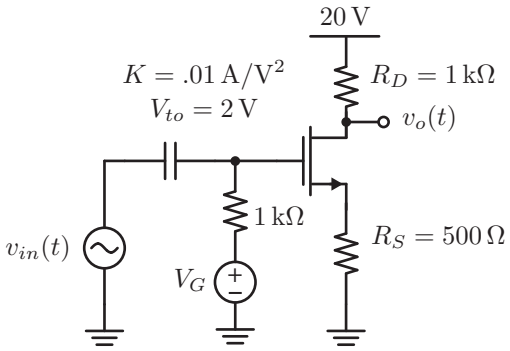
$$g_m = 2K(V_{GS} - V_{to}) = 2\sqrt{KI_{DS}} \tag{1}$$

Given that Tony has demanded $g_m = 20\,\text{mS}$ $(0.02\,\text{S})$, find the necessary bias V_G that should be applied at the gate to achieve this.

$$g_m = .02 = 2\sqrt{KI_{DS}} = 2\sqrt{.01I_{DS}} \Rightarrow I_{DS} = .01\,\text{A}$$

$$V_S = I_{DS}R_S = (.01\,\text{A})(500\,\Omega) = 5\,\text{V}$$

$$g_m = .02 = 2K(V_{GS} - V_{to}) = 2(.01)(V_G - 5 - 2) \Rightarrow \boxed{V_G = 8\,\text{V}}$$

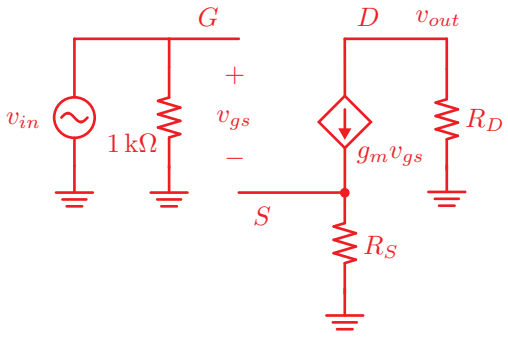


(b) *(12 points)* Draw the equivalent small-signal model of the circuit and show that the gain is given by

$$A_v = \frac{v_o}{v_{in}} = \frac{-g_m R_D}{1 + g_m R_S} = -\frac{20}{11} \approx -2 \tag{2}$$

Be sure to label all components and values.

The SS model of this circuit is shown below.



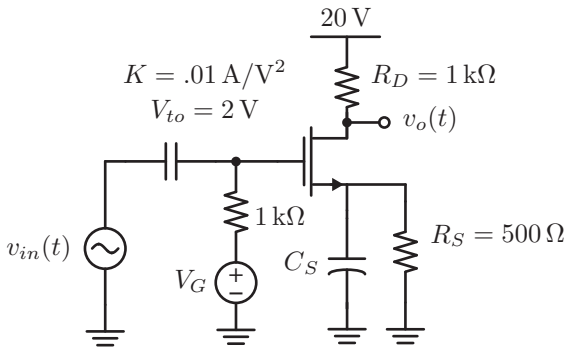
Now we proceed to find the small-signal gain of this amplifier.

$$v_s = g_m v_{gs} R_S = g_m R_S (v_{in} - v_s) \Rightarrow v_s = \frac{g_m R_S}{1 + g_m R_S} v_{in}$$

$$v_o = -g_m v_{gs} R_D = -g_m R_D (v_{in} - v_s) = -g_m R_D \left(v_{in} - \frac{g_m R_S}{1 + g_m R_S} v_{in} \right) = -g_m R_D \left(\frac{1}{1 + g_m R_S} \right) v_{in}$$

$$\boxed{\frac{v_o}{v_{in}} = \frac{-g_m R_D}{1 + g_m R_S} = -\frac{20}{11} \approx -2}$$

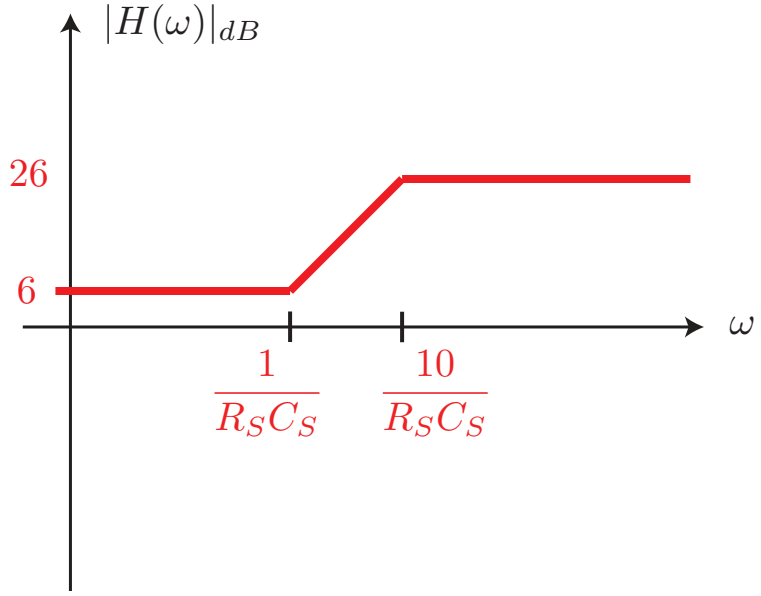
(c) *(8 points)* Tony now insists that the gain be a function of the signal frequency. Jerry cleverly adds in a source capacitor as follows.



The gain of the amplifier now becomes a complex transfer function, given by

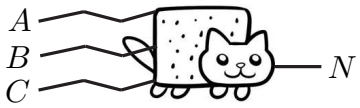
$$H(\omega) = \frac{\mathbf{V}_o}{\mathbf{V}_{in}} = \frac{-g_m R_D}{1 + g_m Z_S} = \frac{-g_m R_D}{1 + g_m R_S}\left(\frac{1 + j\omega R_S C_S}{1 + j\omega \frac{R_S C_S}{1 + g_m R_S}}\right) \approx -2\frac{1 + j\omega R_S C_S}{1 + j\omega R_S C_S/10} \tag{3}$$

Sketch the magnitude Bode plot for the transfer function. Be sure to label any cutoff frequencies and asymptotic magnitude values, as well as slopes. You may leave your plot labels in terms of $R_S C_S$ for convenience. (*Hint:* $20\log_{10}(2) = 6$)



4. **Introducing... the NYAN gate!**

Dennis has finally perfected the NYAN gate and is ready to add it to the current repertoire of logic gates. Its logic gate symbol is shown below:



Unlike most other logic gates, the NYAN gate takes in exactly three inputs. The truth table showing all its possible input/output combinations is as follows:

A	B	C	N
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(a) *(2 points)* Is the NYAN gate commutative? Briefly justify why or why not.

No, it is not. Observe that the order of inputs into the gate actually matters. For example, NYAN(0, 0, 1) $\neq$ NYAN(0, 1, 0).

(b) *(6 points)* Write the SOP Boolean expression for the output N in terms of the inputs A, B, and C. Simplify it into a sum of two terms only.

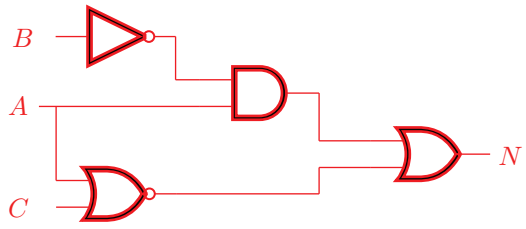
$$\begin{aligned} N &= \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C \\ &= \overline{A}\,\overline{C}(B + \overline{B}) + A\overline{B}(\overline{C} + C) \\ &= \overline{A}\,\overline{C} + A\overline{B} \end{aligned}$$

(c) *(8 points)* Implement your simplified expression from above with a logic gate circuit. Clearly indicate the inputs A, B, and C, as well as the output N. For **full** credit, use no more than 4 logic gates.

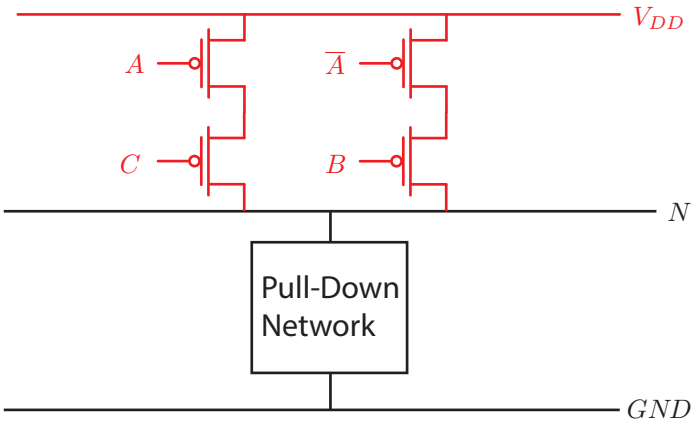
The first term can be rewritten as a NOR using De Morgan's law:

$$\overline{A}\,\overline{C} = \overline{A + C}$$

Then the logic gate circuit can be implemented as follows:

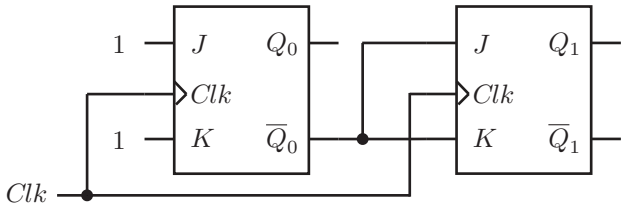


(d) *(4 points)* Now help Dennis implement the NYAN gate using CMOS digital logic. He already has the pull-down network in; your job is to fill in the *pull-up network* above it. For **full** credit, use no more than 4 transistors (you may use inverted inputs).



5. **The Final Countdown**

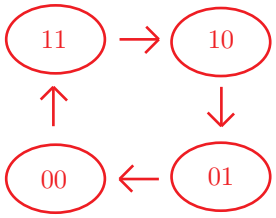
The hours that you have left in EE42/100 are numbered, and you can't wait to finish this exam and GTFO to party away your Friday night and what's left of summer. But before you do so, you must help finish our timer circuit below to perform the final countdown.

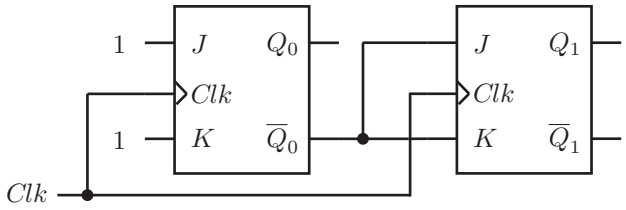


Recall that the behavior of the JK flip flop is as follows:

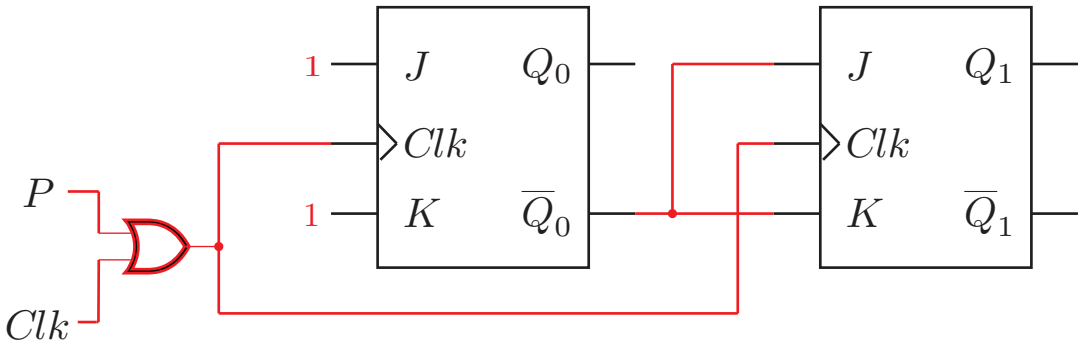
Clk	J	K	Q_{n+1}
0	×	×	Q_n
1	×	×	Q_n
↑	0	0	Q_n
↑	0	1	0
↑	1	0	1
↑	1	1	$\overline{Q}_n$

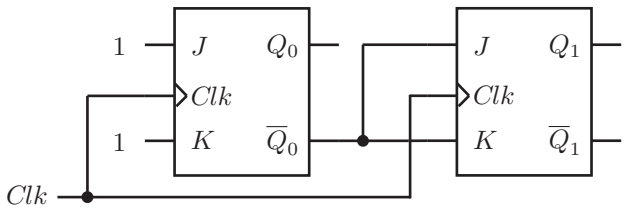
(a) *(4 points)* The output of this circuit is given by $Q = (Q_1Q_0)_2$. Draw the state transition diagram for the given circuit above.



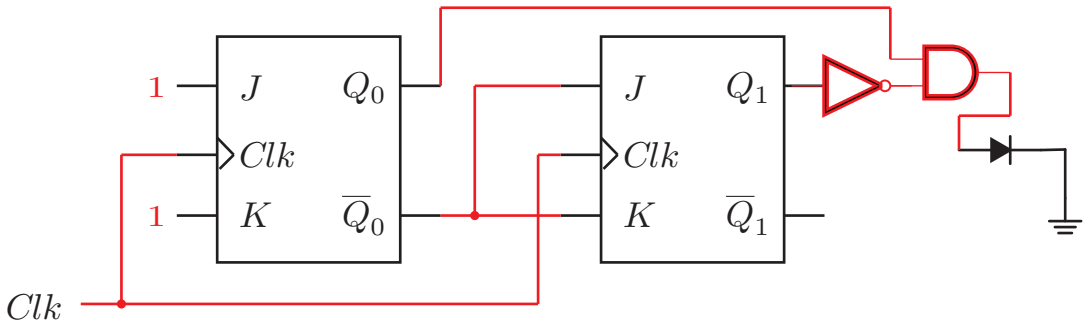


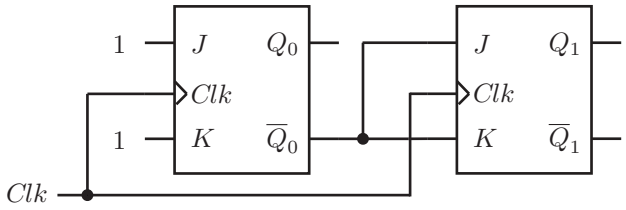
(b) *(4 points)* The first feature we want to add is the ability to pause the timer. Suppose we add in a new input P; when $P = 1$, the timer keeps its current state and ignores the clock (Q should *not* reset to 0). Then when $P = 0$, the timer continues as usual. Given the original two flip flops below, make all the necessary connections to implement this new feature, using logic gates if necessary.





(c) *(4 points)* Suppose the next feature we want to add is an LED (light-emitting diode) such that it lights up whenever our timer lands on the state $Q = 01_2$. The LED lights up when the signal line feeding into it is high (or 1). Make all the necessary connections to implement this new feature, using logic gates if necessary.





(d) *(8 points)* You may have noticed that our timer doesn't have a very wide range, since it only has two bits of output. The last extension we want to do is to modify the timer so that it counts down from $Q = 7$. Make all the necessary connections to implement this new feature, using logic gates if necessary. (Notice that we have drawn in a third flip flop for you.)