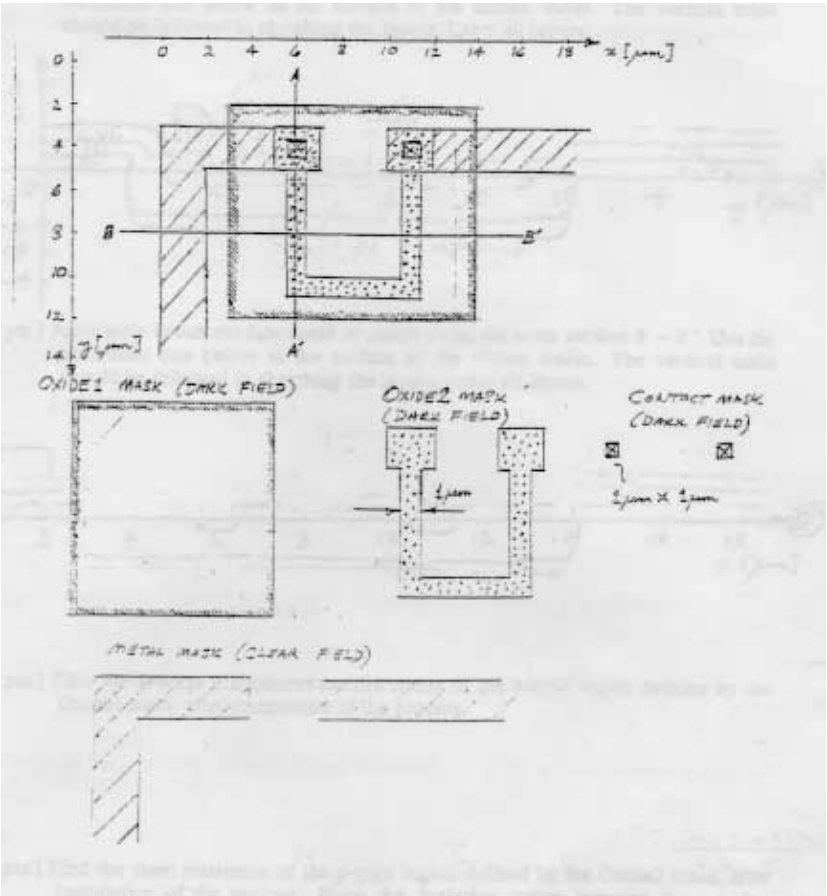
EE 105
Midterm #1
Spring 1998

Problem #1: Resistor Layout [18 points]

The CAD layout for a resistor is shown below, along with the individual mask layers. For the Oxide1 mask, the *interior* of the rectangle is filled in ("colored") on the *CAD layout*.



Process Flow

0. Starting material: p-type silicon wafer, *Na = 10^16 / cm^3*

1. Grow 0.5 micrometers of thermal SiO2 and pattern using the **Oxide1 mask.**

2. Implant phosphorus (dose Qd = 5 x 10^12 / cm ^2) and anneal. The junction depth is Xj,1 = 1.5 micrometers with the p-type substrate. The phosphorus does not penetrate the oxide.

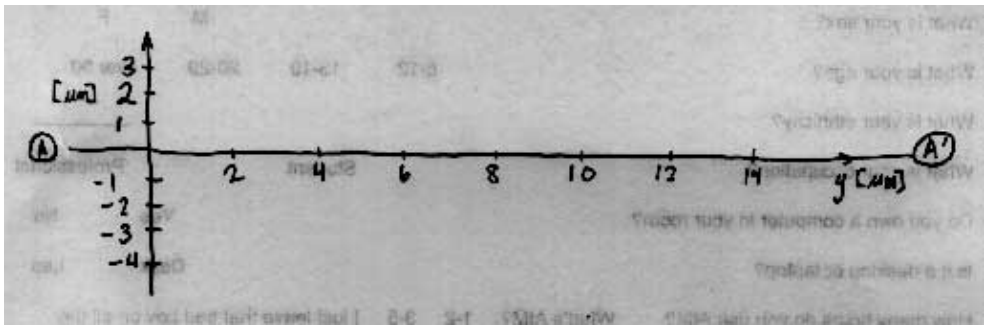
3. Deposit 0.5 micrometers of CVD SiO2 and pattern using the **Oxide2 mask**.

4. Implant boron (dose Qa = 1.5 x 10^12 / cm^2) and anneal to obtain a junction depth Xj,2 = 0.5 micrometers with the n-type region formed in step 2. The boron does not penetrate the 0.5 micrometer thick CVD oxide. During this anneal, the phosphorus penetrates further into the substrate and its junction depth with the substrate increases to Xj,1 = 2 micrometers.

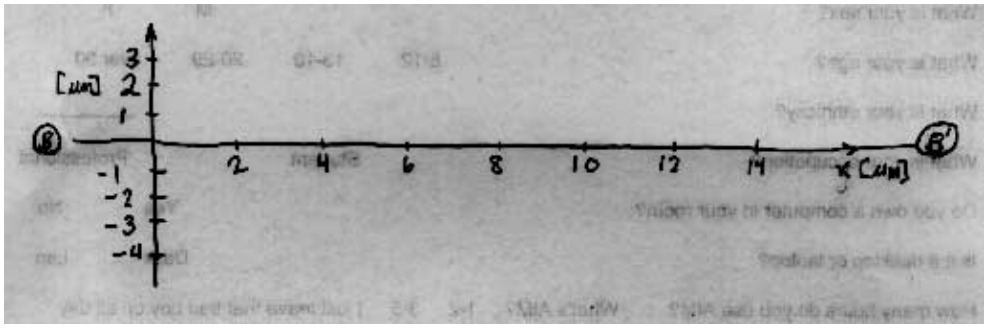
5. Deposit 0.5 micrometers of CVD SiO2 and pattern using the **Contact mask**.

6. Deposit 1 micrometer of aluminum and pattern using the **Metal mask**.

(a) [6 pts.] Accurately sketch the fabricated structure along the cross section A - A'. Use the horizontal line below as the surface of the silicon wafer. The vertical scale should be followed in sketching the layers. Label all layers.



(b) [6 pts.] Accurately sketch the fabricated structure along the cross section B - B'. Use the horizontal line below as the surface of the silicon wafer. The vertical scale should be followed in sketching the layers. Label all layers.

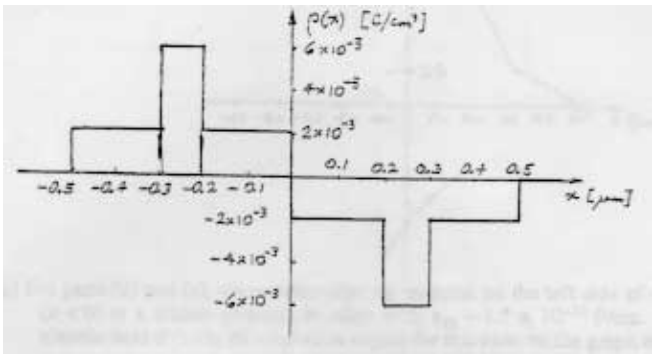


(c) [3 pts.] Find the average phosphorus concentration in the n-type region defined by the Oxide1 mask, after completion of the process.

(d) [3 pts.] Find the sheet resistance of the p-type region defined by the Oxide2 mask, after completion of the process. Note: the depletion region between the p and n regions penetrates 0.1 micrometers into the p-type layer.

Problem #2: Junction Electrostatics [17 points]

The depletion region in a p-n junction under a particular reverse bias voltage has a charge density given by

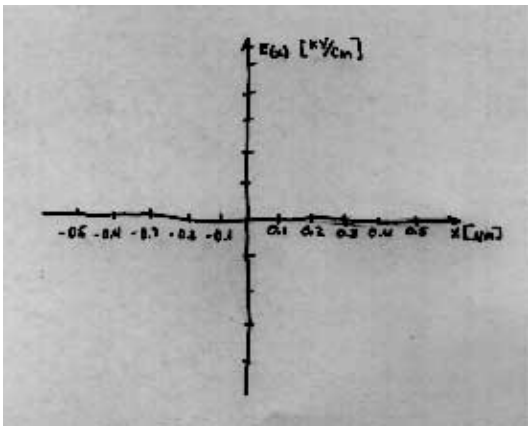


Given:
q = 1.6 x 10^-19 C, Permittivity = 1.05 x 10^-12 F/cm, 1 micrometer = 10^-4 cm

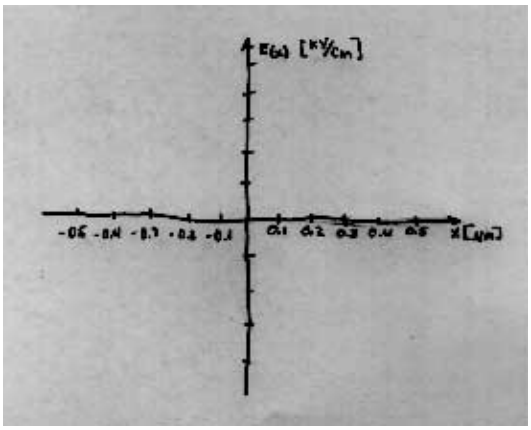
(a) [2 pts.] Which side of the junction (left, x < 0 or right, x > 0) is n-type and why?

(b) [4 pts.] Find the numerical value of the electric field at x = 0 in kV/cm, assuming that the material is silicon.

(c) [4 pts.] Plot the electric field *E(x)* in the depletion region on the graph below, assuming that the material is silicon throughout.



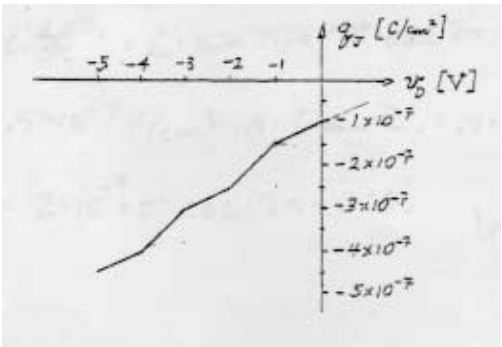
(d) [4 pts.] For parts (d) and (e), we consider that the material on the left side of the junction (x < 0) is a silicon-germanium alloy with permittivity = 1.5 x 10^-12 F/cm. Replot the electric field *E(x)* in the depletion region for this case on the graph below.



(e) [3 pts.] Find the numerical value of the depletion capacitance per area of the reverse biased silicon-germanium/silicon junction.

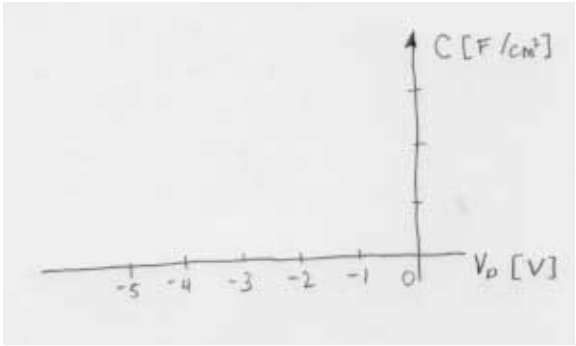
Problem #3: New junction capacitor [15 points]

The charge per unit area in a specially designed junction capacitor is given below.



(a) [3 pts.] What is the numerical value of the capacitance per unit area for Vd = 0 V for this charge-storage element?

(b) [5 pts.] Plot the capacitance per unit area as a function of the DC bias voltage Vd on the graph below.



(c) [4 pts.] For a junction area of 10 micrometers by 20 micrometers and a bias voltage Vd = -2.5 V, find the small-signal current *i(t)* into the junction capacitor for a small-signal voltage of *Vd(t)* = 10 mV sin (2*pi*10^6 *t*).

(d) [3 pts.] What is the maximum amplitude of the the sinusoidal voltage *Vd(t)* for the small-signal approximation to remain accurate, at the bias voltage in part (c). Justify your answer.

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