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6:30-8:00pm

EECS 141: FALL 2001—MIDTERM 1

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):
NMOS:
$V_{Tn} = 0.4$, $K'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$
PMOS:
$V_{Tp} = -0.4V$, $K'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last SOLUTIONS First

GRAD/UNDERGRAD	

Problem 1: ____/ 8

Problem 2: ____/12

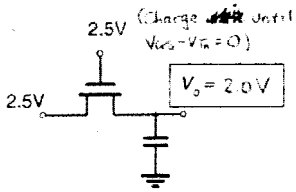
Problem 3: ____/12

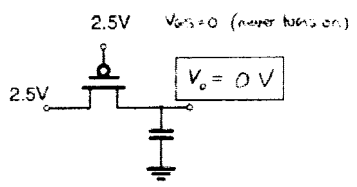
Problem 4: ____/12

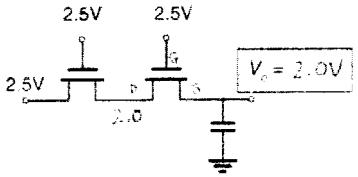
Total: ____/44

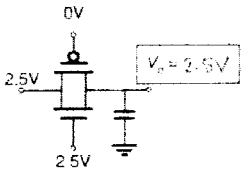
PROBLEM 1. MOS transistor as a switch

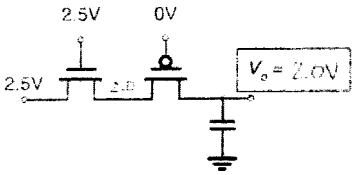
Find the final value of the voltage V_o. Assume $V_{TN} = |V_{TP}| = 0.5V$. Assume that the capacitor is initially discharged, and ignore subthreshold conduction and body effect.

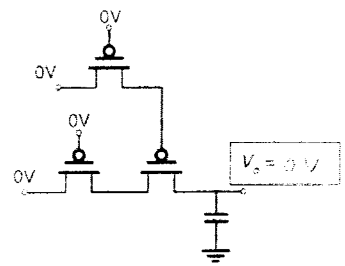


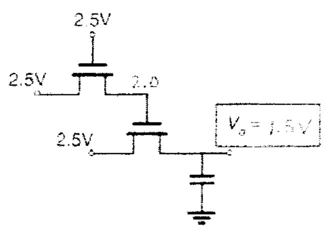


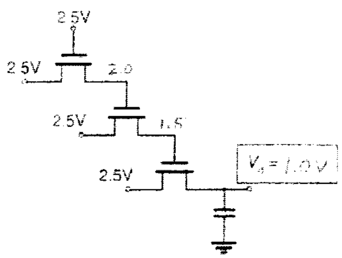












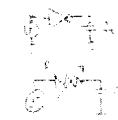
PROBLEM 2. Equivalent RC models.

In class we modeled the inverter delay by finding its equivalent resistance and capacitance. You are asked to find the equivalent resistance and input capacitance of a capacitively loaded symmetrically sized inverter.

a) Draw a schematic of how you would measure the equivalent resistance and briefly explain how would you do this.

circuit 1

circuit 2



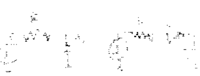
Measure delay through both circuits, and change variable resistor in circuit 2 until delays are equal.

⇒ R = Req

b) Draw a schematic of how you would measure the equivalent input capacitance of this inverter. Explain the measurement procedure.

Measure the voltage at the input ...

OR



Same as (a), measure delay ...

c) Does the input capacitance of this inverter depend on its loading? Explain your answer. YES.

When both terminals of input capacitance ... are changing in opposite directions, the capacitance becomes larger (Miller multiplication). If the loading on the output is large, the output voltage will change only slightly in the time it takes the input to completely change, so no Miller effect occurs.

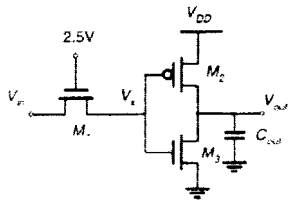
d) Does the input capacitance of this inverter depend on the type of transition (H-L or L-H transition)? If the answer is yes, which one is larger? Explain your answer.

$C_{in} = C_{ox} (W_n L_n K_{eqn} + W_p L_p K_{eqp})$

Since ... ⇒ $C_{HL} > C_{LH}$

PROBLEM 3. Gate delays.

Consider a three-transistor circuit as shown in the figure below. V_{DD} = 2.5V and input signal switches between 0 and V_{DD} with sharp rise and fall times. Use the transistor parameters indicated on the first page of the midterm. Ignore body effect. All transistors are minimum length, L = 0.25μm. Transistor widths: W_2 = 2μm, W_3 = 1μm.



a) Find the M_3 transistor width such that the switching point of the inverter (V_M) is placed in the middle of the V_X signal swing.

$V_{in} = 2.5V \rightarrow V_x = V_{OL} = 2.5 - 0.4 = 2.1V$

$V_{in} = 0 \rightarrow V_x = 0V$

$V_m = \frac{V_{OH} - V_{OL}}{2} = 1.05V$

At $V_{in} = V_m$, $V_{DS} = -1.45V$ for PMOS M_2 and $V_{DS} = 1.05V$ for NMOS M_3, which means both M_2 and M_3 are velocity saturated ($V_{DSATP} = -1$, $V_{DSATN} = 0.6$).

We know for the inverter $I_{M2} = I_{M3}$, so we can solve for the width of M_3 using the velocity saturated current equations.

$$\frac{I_{DS3}}{I_{DS2}} = \frac{W_n k_n' V_{DSATn}\left(V_m - V_{tn} - \frac{V_{DSATn}}{2}\right)}{W_p k_p' V_{DSATp}\left((V_{DD} - V_m) + V_{tp} + \frac{V_{DSATP}}{2}\right)} = 1$$

$$\Rightarrow \frac{W_n}{W_p} = \frac{k_n' V_{DSATn}\left(V_m - V_{tn} - \frac{V_{DSATn}}{2}\right)}{k_p' V_{DSATp}\left((V_{DD} - V_m) - V_{tp} - \frac{V_{DSATP}}{2}\right)} = 1.46 \quad \left| W_n = \frac{W_p}{1.46} = 1.37\mu m \right.$$

b) Find the t_{pLH} delay of this circuit. C_{ox} = 6fF/μm². Overlap capacitances are C_o = 0.3 fF/μ. Bottom-plate PN junction capacitances are 2fF/μ (drain lengths are included). Ignore the sidewall capacitances. Ignore the impact of rise/fall times on propagation delay. C_{out} = 10fF.

$t_{pLH} = t_{p1} + t_{p2} = 0.69\left(R_{eq1}C_{eq1} + R_{eq2}C_L\right)$

t_{p1}: $R_{eq1} = \frac{1}{2}\left[\frac{V_{DD} - V_{tn}}{I_{DSAT_1}} + \frac{V_{DD}/2}{I_{DSAT_1}}\right] = \frac{3}{4}\frac{V_{DD}}{I_{DSAT_1}} = \frac{3}{8}\frac{V_{DD}}{I_{DSAT_1}}$

where $I_{DSAT_1} = k_n'\left(\frac{W_1}{L}\right)\left[(V_{DD} - V_{tn})V_{DSATn} - \frac{V_{DSATn}^2}{2}\right]$

$C_{eq1} = C_{ox}L\left(W_1 + \frac{1}{3}W_{P2}\right) + C_o\left(W_3 + W_{P2}\right) + C_{bottom\ plate}W_1$

t_{p2}: $R_{eq2} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT_2}}$

where $I_{DSAT_2} = \left[k_p'\left(\frac{W_2}{L}\right)\left[(V_{DD} - V_{tp})V_{DSATP} - \frac{V_{DSATP}^2}{2}\right]\right]$

$C_L = C_{out} + \sum_{MILLER} 2C_o\left(W_{N3} + W_{P2}\right) + C_{bottom\ plate}\left(W_{N3} + W_{P2}\right)$

$I_{DSAT_1} = 500\mu A \quad C_{eq1} = 7.8fF$

$R_{eq2} = 3.35k\Omega$

$t_{p1} = 0.69\left(3.35k\Omega\right)\left(7.8fF\right) = 18ps$

$I_{DSAT_2} = 384\mu A \quad C_{eq2} = 18.8fF$

$R_{eq2} = 4.88k\Omega$

$t_{p2} = 0.69\left(4.88k\Omega\right)\left(18.8fF\right) = 63ps$

$t_{pLH} = t_{p1} + t_{p2} = \boxed{81\ ps}$

PROBLEM 4. Wire modeling.

Consider an isolated 2mm long and 1um wide M1 wire over a silicon substrate driven by an inverter with zero output resistance and capacitance

a) If the wire width is doubled, the delay of this wire will be (circle one):

More than 2x shorter / Exactly 2x shorter / (Shorter, but less than 2x) /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation: Delay depends on wire resistance, parallel plate capacitance, and fringing Cff. Initially, $t \approx R(C_p + C_f)$. After doubling width, $t' \approx \frac{R}{2}(2C_p + C_f) = R(C_p + \frac{C_f}{2})$

b) If the wire length is halved, the delay of this wire will be (circle one):

(More than 2x shorter) / Exactly 2x shorter / Shorter, but less than 2x /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation: After length is halved, $t' \approx \frac{R}{2}(\frac{C_p}{2} + \frac{C_f}{2}) = \frac{1}{4}R(C_p + C_f)$

c) If the wire thickness is doubled, the delay of this wire will be (circle one):

More than 2x shorter / Exactly 2x shorter / (Shorter, but less than 2x) /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation: After thickness is doubled, $t' \approx \frac{R}{2}(C_p + xC_f)$ where x is larger than 1, but not much more than 2.

d) If the oxide thickness (between the wire and the substrate) is doubled, the wire delay will be (circle one):

More than 2x shorter / (Exactly 2x shorter) / Shorter, but less than 2x /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation: After oxide thickness is doubled, the relative magnitude of parallel-plate and fringing capacitances change, [illegible] depending on the wire geometry. The wire resistance does not change. To first approximation we can claim that both C_p and C_f are halved, or $t' \approx R(\frac{C_p}{2} + \frac{C_f}{2})$.