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6:30-8:00pm

EECS 141: FALL 2007—MIDTERM 1

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS:
$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{VSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2|\Phi_F| = 0.6V$
PMOS:
$|V_{Tp}| = 0.4V$, $|k'_p| = 30\ \mu A/V^2$, $|V_{VSAT}| = 1V$, $\lambda = 0$, $|\gamma| = 0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last Solutions First

GRAD/UNDERGRAD	

Problem 1: _____/ 26

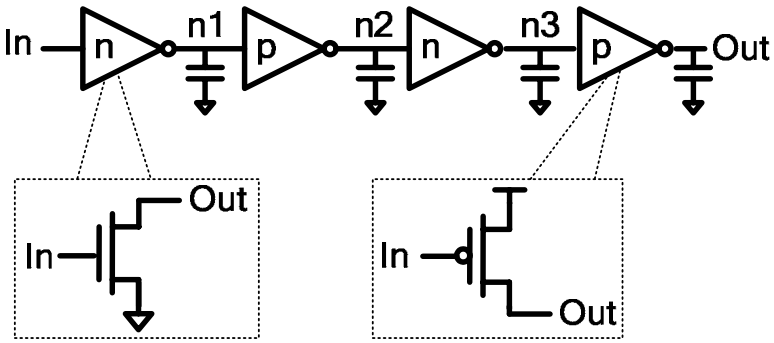
Problem 2: _____/ 16

Problem 3: _____/ 10

Total: _____/ 52

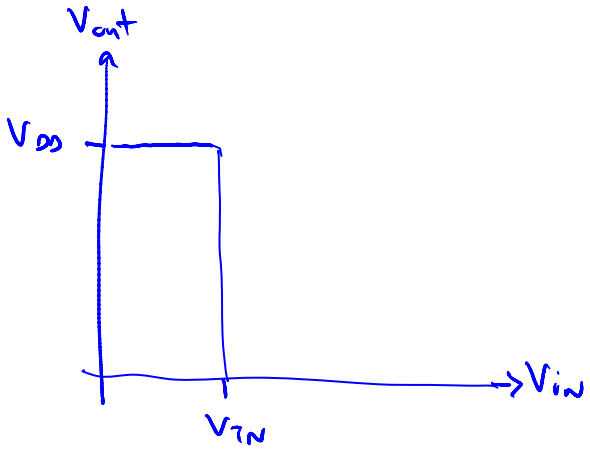
PROBLEM 1. (26 pts) Dynamic Inverters: VTC and Delay.

For this problem only, you should assume that $R_{sq,p} = R_{sq,n} = R_{sq}$. In other words, an inverter with $W_p = W_n = 1\mu m$ would have equal rising and falling delays. Note that this means that $t_{inv} = 2 \cdot \ln(2) \cdot L \cdot R_{sq} \cdot C_G$. Also, $V_{DD} = 2.5V$.



The figure above shows a chain of 4 dynamic "inverters"; every cycle, before the inverters are used, their outputs are set to a well-known state through transistors not shown here (which you can assume are negligibly small compared to the transistors in the inverter). Specifically, for an "n" dynamic inverter, its output starts at V_{DD} (2.5V), and for a "p" dynamic inverter the output starts at Gnd (0V). So, in the figure above, nodes "n1" and "n3" would be initially charged to V_{DD}, and nodes "n2" and "Out" would be initially discharged to Gnd (0V). Once these initial voltages have been set, no transistors drive the output until there is a rising transition at the input of an n inverter, or a falling transition at the input of a p inverter. In other words, the inverter's output voltage is simply stored on the capacitance at its output.

a) **(3 pts)** Please draw the VTC of an n dynamic inverter as its input is swept from 0V to V_{DD}. Remember that the output of an n inverter is initially charged to V_{DD}. Please also provide the values of V_{OH}, V_{OL}, V_{IH}, and V_{IL}.



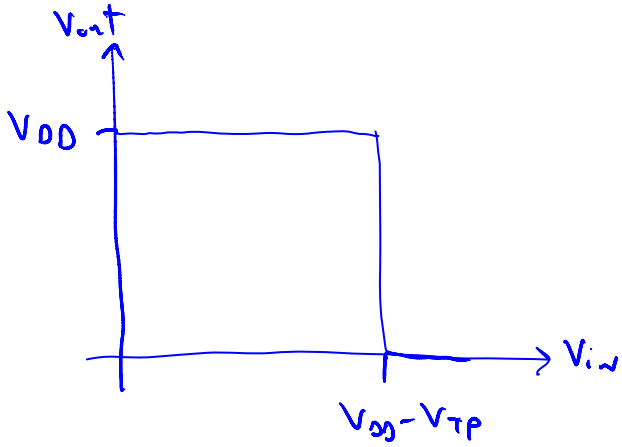
$V_{OH} = V_{DD} = 2.5V$

$V_{OL} = 0V$

$V_{IH} = V_{TN} = 0.4V$

$V_{IL} = V_{TN} = 0.4V$

b) **(3 pts)** Please draw the VTC of a p dynamic inverter as its input is swept from V_{DD} to 0V. Remember that the output of a p inverter is initially discharged to Gnd. Please also provide the values of V_{OH}, V_{OL}, V_{IH}, and V_{IL}.



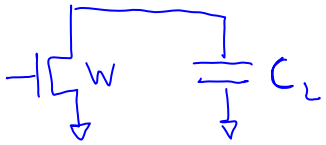
$V_{OH} = V_{DD} = 2.5V$

$V_{OL} = 0V$

$V_{IH} = V_{DD} - V_{TP} = 2.1V$

$V_{IL} = V_{DD} - V_{TP} = 2.1V$

c) **(4 pts)** Now we'll look at the sizing of a chain of such dynamic inverters. Using the RC model, write an equation for the delay of an n inverter of width W driving a fixed capacitance C_L with a rising step (0 → V_{DD}) at its input. Your expression for the delay should be in terms of W, L, R_{sq}, C_L, C_G (effective gate capacitance per µm of width), and C_D (effective diffusion capacitance per µm of width).



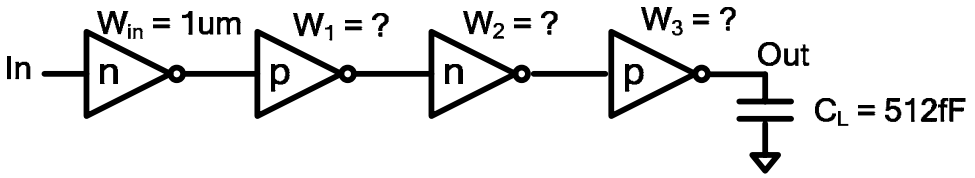
$C_{tot} = C_L + WC_D$

$R_{inv} = R_{sq} \cdot \frac{L}{W}$

$t_p = \ln(2) R_{sq} \cdot \frac{L}{W} \cdot (C_L + WC_D)$

$t_p = \ln(2) R_{sq} L \left(\frac{C_L}{W} + C_D \right)$

$$\boxed{t_p = \ln(2) L R_{sq} C_G \left(\frac{C_L}{W C_G} + \frac{C_D}{C_G} \right)}$$



d) **(6 pts)** Noting that the delay of a p inverter will follow the same equation you derived in part c) for the delay of an n inverter, and assuming C_G = 1.5fF/µm, size the buffer chain shown above to minimize its delay from In rising to Out rising.

$C_{in} = 1.5\,fF$

$C_L/C_{in} = 512fF/1.5fF = 341.33$

$f = \sqrt[4]{C_L/C_{in}} = 4.298 \approx 4.3$

$W_1 = f\,W_{in}$

$W_2 = f^2\,W_{in}$

$W_3 = f^3\,W_{in}$

Width	Value (µm)
W_1	4.3
W_2	18.49
W_3	79.5

e) **(4 pts)** Using your sizing and assuming $\gamma = C_D/C_G = 0.5$, what is the delay of this inverter chain? Please provide your delay in units of $t_{inv} = 2\cdot\ln(2)\cdot L\cdot R_{sq}\cdot C_G$.

$t_p = N\,t_{dinv}\,(\gamma + f)$

$t_{dinv} = \ln(2)\,R_{sq}\,C_G\,L = \frac{1}{2}\,t_{inv}$

$t_p = 4 \cdot \frac{t_{inv}}{2} \cdot (0.5 + 4.3)$

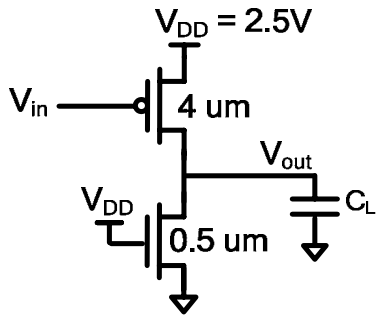
$\boxed{t_p = 9.6\,t_{inv}}$

f) **(6 pts)** For a constant C_L/C_{in}, would the optimum number of stages for minimum delay with standard inverters be larger, smaller, or the same as the optimum number of stages for a chain of these dynamic inverters? Which chain would have lower delay? Be sure to explain your answers. If you are unsure about the answers to this question, you may want to complete the rest of exam and come back to this later.

The number of stages would stay the same, because N is set only by C_L/C_{in} and γ – neither of which have changed. The delay of the dynamic inverter chain would be half the delay of the standard chain though, because $t_{dinv} = \frac{1}{2} t_{inv}$.

PROBLEM 2. (16 pts) IV Characteristics and Power Consumption

For this problem, all transistors are minimum channel length (i.e., L = 0.25µm).



a) **(6 pts)** Using the unified transistor IV model, how much current flows from V_{DD} to Gnd when V_{in} = 0V? (Hint: Think about the regions of operation – which transistor would have more current if both devices were velocity saturated?)

Since $W_p >> W_N$, if both transistors were velocity saturated, the PMOS would have more current. So, in order for I_{DP} to equal I_{DN}, the PMOS can not be velocity saturated (it will be linear). The NMOS device will be velocity saturated, and therefore it sets the current:

$$I_0 = 115\mu A/V^2 \cdot \frac{0.5\mu m}{0.25\mu m} \cdot 0.6V \cdot \left(2.5V - 0.4V - \frac{0.6V}{2}\right)$$

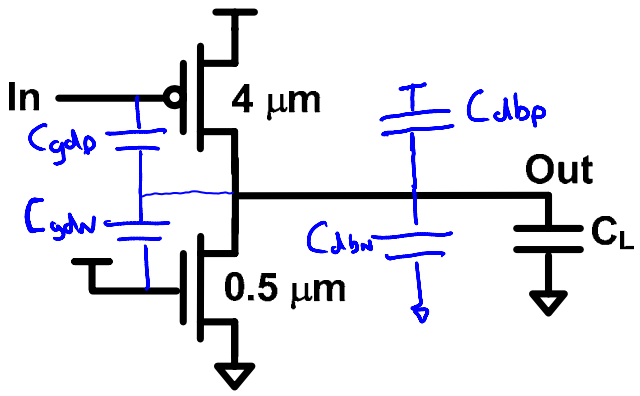
$$\boxed{I_0 = 248.4\mu A}$$

b) **(6 pts)** Using the detailed model of transistor capacitance discussed in Lecture 7, please draw all of the capacitors connected to Out when $V_{in} = V_{DD}$ on the figure below. You should also write out the equations you would use to calculate the values of these capacitors – these equations should be in terms of C_{ox}, C_{ov}, L, L_S, $C_{j,bottom}$, $C_{j,sidewall}$, $C_{j,gate\_edge}$, and the widths of the transistors. (Note that you do not need to plug in any numbers for these parameters – only write out the equations.)

$I_N = V_{DD}$, Out = 0V

PMOS cutoff

NMOS linear



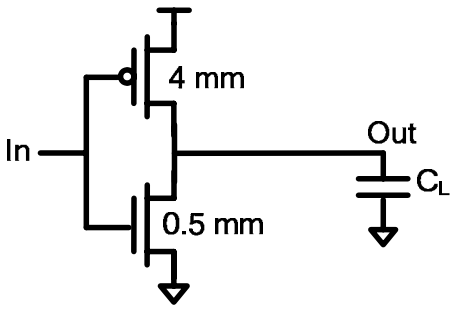
$C_{gdp} = 4\mu m \cdot C_{ov}$

$C_{gdn} = 0.5\mu m \cdot \left(C_{ov} + \frac{LC_{ox}}{2}\right)$

$C_{dbp} = 4\mu m \cdot C_{j,gate\_edge} + 4\mu m \cdot L_S \cdot C_{j,bottom} + (4\mu m + 2L_S) C_{j,sidewall}$

$C_{dbn} = 0.5\mu m \cdot C_{j,gate\_edge} + 0.5\mu m \cdot L_S \cdot C_{j,bottom} + (0.5\mu m + 2L_S) \cdot C_{j,sidewall}$

c) **(4 pts)** Now using the simplified capacitance model with C_G = 2fF/μm and C_D = 1fF/μm, how much dynamic power would a standard CMOS inverter with the same sizing (shown below) consume if In transitions from 0 to 1 every other clock cycle, the clock frequency is 100MHz, and C_L = 30fF? Don't forget to include the power consumption from driving the inverter's input capacitance.



$C_{switched} = C_L + 4.5\mu m\, C_D + 4.5\mu m\, C_G$

$C_{switched} = 43.5\ fF$

$P = \alpha_{0\to1} C_{switched} V_{DD}^2 f$

$P = \frac{1}{2} \cdot 43.5\ fF \cdot (2.5\ V)^2 \cdot 100\ MHz$

$P \approx 13.59\ \mu W$

PROBLEM 3. (10 pts) Scaling.

a) **(5 pts)** Let's assume that the capacitive load that sets the delay of an inverter is C_L, where $C_L = WLC_{ox} + C_f$, and C_f does not scale with technology. If in a 90nm technology WLC_{ox} is equal to C_f, what would WLC_{ox} be (in terms of C_f) in a 65nm technology?

WLC_{ox} scales as $\frac{1}{S} \cdot \frac{1}{S} \cdot S = \frac{1}{S}$

So: $(WLC_{ox})_{65nm} = \frac{65}{90} \cdot (WLC_{ox})_{90nm}$

$$\boxed{(WLC_{ox})_{65nm} = \frac{65}{90} C_f}$$

b) **(5 pts)** Given your answer to part a), how would the delay of an inverter with this C_L scale from 90nm to 65nm?

$t_p \propto R_{inv} C_L$

R_{inv} is constant with scaling

$C_{L\,90nm} = (WLC_{ox})_{90nm} + C_f = C_f + C_f$

$C_{L\,65nm} = (WLC_{ox})_{65nm} + C_f = \frac{65}{90} C_f + C_f$

$$\frac{t_{p\,65nm}}{t_{p\,90nm}} = \frac{(1 + 65/90)}{2}$$

$$\boxed{\frac{t_{p\,65nm}}{t_{p\,90nm}} = 0.861}$$