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6:30-8:00pm

EECS 141: FALL 2008—MIDTERM 1

For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

NMOS:
V_{Tn} = 0.2V, μ_n = 400 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, λ = 0
PMOS:
$|V_{Tp}|$ = 0.2V, μ_p = 200 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, λ = 0

NAME	Last Solutions First

GRAD/UNDERGRAD	

Problem 1: _____/ 18

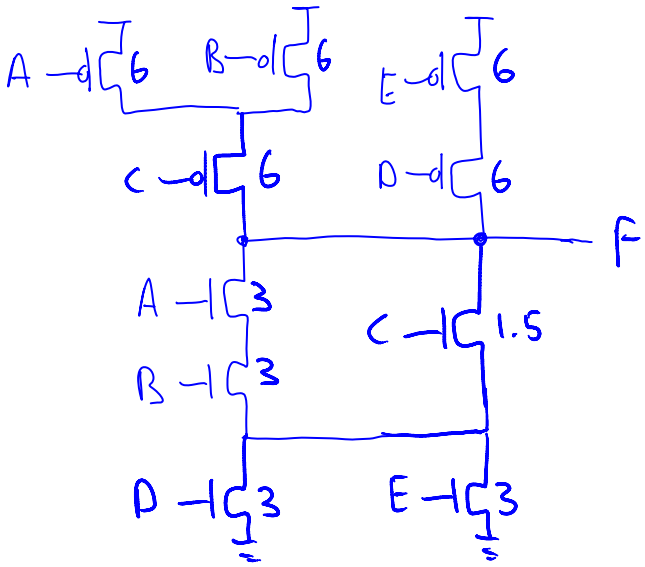
Problem 2: _____/ 20

Problem 3: _____/ 26

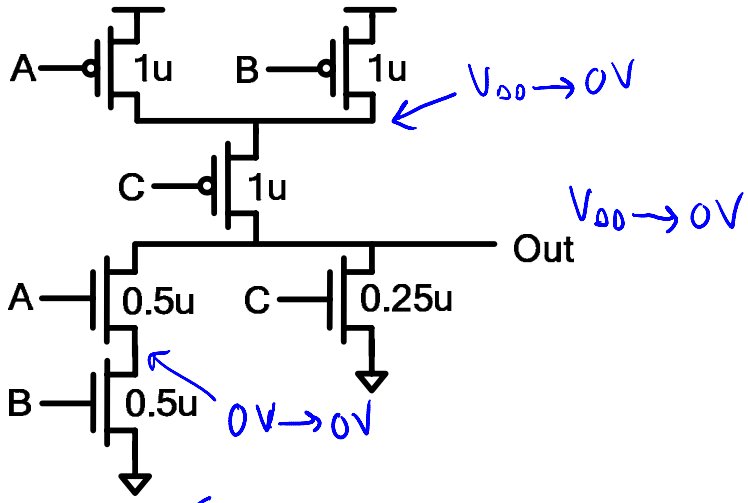
Total: _____/ 64

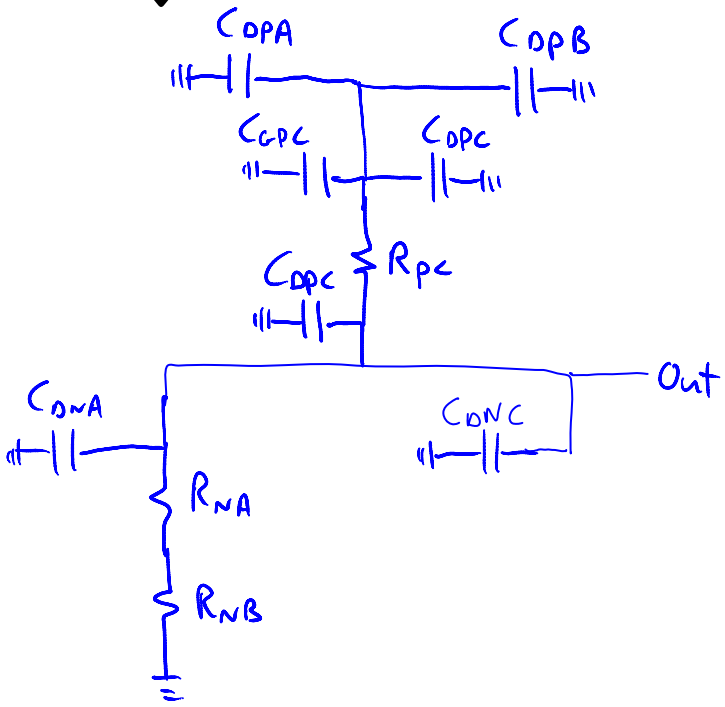
PROBLEM 1. (18 pts) Complex Gates and Elmore Delay.

a) **(6 pts)** Implement the function $F = \overline{(A \cdot B+C) \cdot (D+E)}$ with a complex static CMOS gate. Assuming $R_{sqp} = 3R_{sqn}$, you should size your gate so that the worst-case pull up resistance is equal to the worst-case pull-down resistance.



b) **(6 pts)** Using the switch model for the transistors, draw the RC network you would use to calculate the delay of the gate shown below when B = V_{DD}, C = 0V, and A transitions from 0V to V_{DD}. You can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10k\Omega/\square$, and $R_{sqp} = 30k\Omega/\square$.





$R_{NB} = R_{NA} = 10k\Omega \cdot \frac{.1\mu m}{.5\mu m} = 2k\Omega$

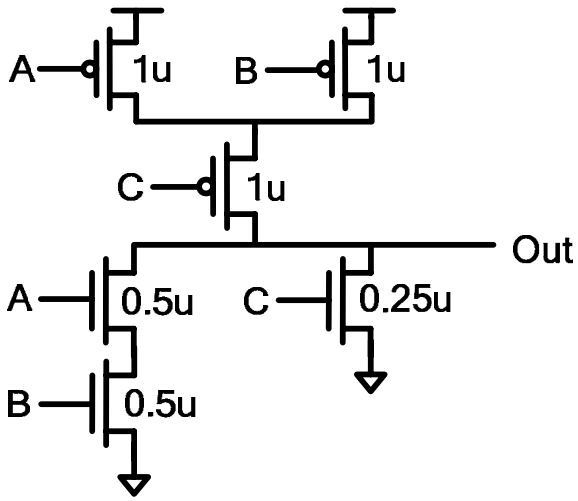
$C_{DNA} = 2fF/\mu m \cdot 0.5\mu m = 1fF$

$C_{DNC} = 2fF/\mu m \cdot 0.25\mu m = 0.5fF$

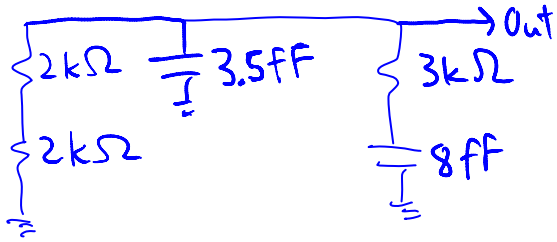
$C_{DPC} = C_{DPB} = C_{DPA} = C_{GPC} = 2fF$

$R_{PC} = 30k\Omega \cdot \frac{.1\mu m}{1\mu m} = 3k\Omega$

c) **(6 pts)** Using the same model and component values you drew in part b), what is the delay of the gate under the same situation (i.e., when B = V_{DD}, C = 0V, and A transitions from 0V to V_{DD})? You should provide your answer for the delay in both absolute ps and in units of t_{inv}. For your convenience the gate has been repeated below.



Elmore τ:

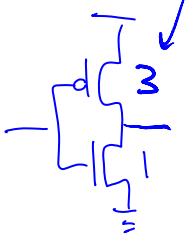


$\tau = 4k\Omega \cdot (3.5fF + 8fF)$

$= 46\,ps$

$t_p = \ln(2) \cdot \tau = 31.885\,ps$

t_{inv}:



$t_{inv} = \ln(2)\, 4 R_{sqN} L C_g = 5.5452\,ps$

$$\frac{t_p}{t_{inv}} = \frac{31.885}{5.5452} = 5.75$$

PROBLEM 2. (20 pts) IV Characteristics, VTCs, and Energy

a) **(2 pts)** For a long-channel (quadratic) NMOS transistor with $V_{GS} = V_{DS} = 1.2V$, how does the drain current change if the mobility of the device μ_n is doubled? How about if C_{ox} is doubled?

In saturation: $I_{DN} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$

So, doubling either μ_n or C_{ox} doubles I_{DN}.

b) **(6 pts)** Now let's look at a short-channel (velocity-saturated) NMOS transistor with $V_{GS} = V_{DS} = 1.2V$. Using the velocity saturated model for this transistor, how much drain current would you get from a 1μm wide transistor if you doubled μ_n to 800 $cm^2/(V \cdot s)$? How about if you doubled C_{ox} to 2.25 $\mu F/cm^2$?

In v-sat: $I_{DN} = W v_{sat} C_{ox} \frac{(V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH} + E_C L)}$

First let's calculate original $E_C = \frac{2 v_{sat}}{\mu_N} = 50\ kV/cm$

So, original $E_C L = 0.5V$ Double μ_N: $E_C L = 0.25V$

Double μ_N:

$I_D = 1\mu m \cdot 1e7\ cm/s \cdot 1.125 \mu F/cm^2 \cdot \frac{(1.2V - 0.2V)^2}{(1.2V - 0.2V + 0.25V)}$

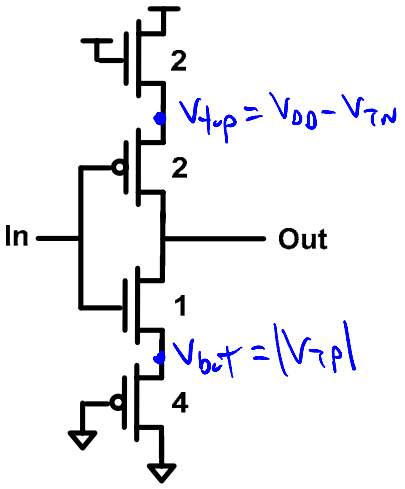
$\boxed{I_D = 900 \mu A}$

Double C_{ox}:

$I_D = 1\mu m \cdot 1e7\ cm/s \cdot 2.25 \mu F/cm^2 \cdot \frac{(1.2V - 0.2V)^2}{(1.2V - 0.2V + 0.5V)}$

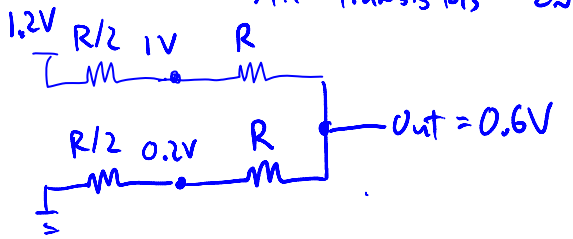
$\boxed{I_D = 1.5\ mA}$

c) **(6 pts)** For parts c) and d), you should use the simple switch model of the transistors with R_{sqn} = 10kΩ/□, R_{sqp} = 20kΩ/□, V_{DD} = 1.2V, and $V_{TN} = |V_{TP}|$ = 0.2V. Draw the VTC of the circuit shown below and provide the values of V_{OH}, V_{OL}, V_{IH}, and V_{IL}.

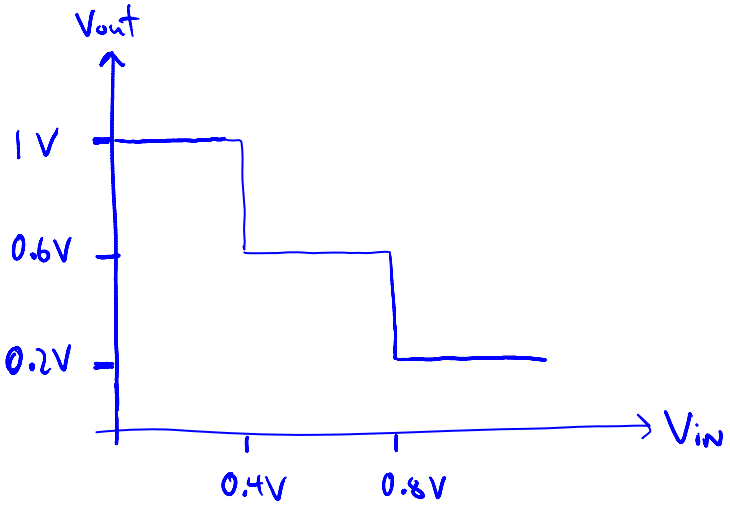


$V_{IN} \le V_{TN} + |V_{TP}|$: Bottom NMOS off
Top PMOS on
$Out = V_{DD} - V_{TN}$

$V_{TN} + |V_{TP}| \le V_{IN} \le V_{DD} - V_{TN} - |V_{TP}|$:
All transistors on:

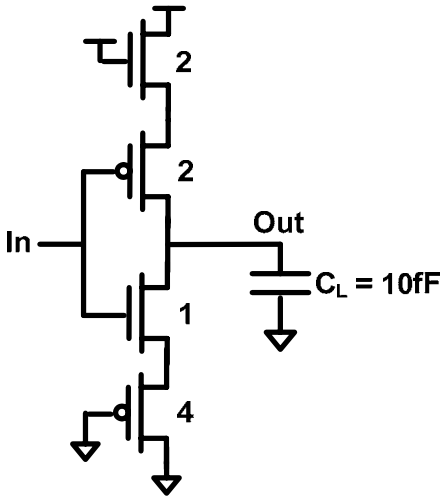


$V_{DD} - V_{TN} - |V_{TP}| \le V_{IN}$: Top PMOS off
Bottom NMOS on
$Out = |V_{TP}|$



$V_{OH} = 1V$
$V_{OL} = 0.2V$
$V_{IH} = 0.8V$
$V_{IL} = 0.4V$

d) **(6 points)** For this same circuit (repeated below), how much energy is supplied by V_{DD} to charge C_L when In steps from V_{DD} to 0V?



When In steps from V_{DD} to 0V, Out goes from $V_{OL} \rightarrow V_{OH}$:

$\Delta V = 1V - 0.2V = 0.8V$

So, charge pulled from supply is:

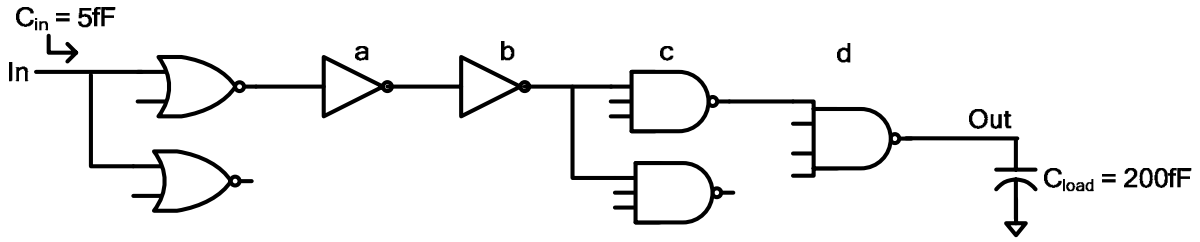
$Q = C_L \cdot \Delta V = 10fF \cdot 0.8V = 8fC$

and:

$E = V_{DD} \cdot Q = 1.2V \cdot 8fC$

$\boxed{E = 9.6fJ}$

PROBLEM 3. Logical Effort and Gate Sizing (26 points)



a) **(6 pts)** What is the path effort from In to Out?

$PE = \Pi LE \cdot \Pi B \cdot F$

$F = 200fF / 5fF = 40 \quad \Pi B = 2 \cdot 2 = 4 \quad \Pi LE = \frac{5}{3} \cdot \frac{5}{3} \cdot 2 = \frac{50}{9}$

$PE = 8000/9 = 888.89$

b) **(2 pts)** What EF/stage minimizes the delay of this chain of gates?

$EF_{opt} = \sqrt[5]{PE} \qquad EF_{opt} \approx 3.888$

c) **(8 pts)** Size the gates to minimize the delay from In to Out.

$\frac{200fF}{d} \cdot 2 = 3.888 \qquad d \approx 102.88\,fF$

$\frac{d}{c} \cdot \frac{5}{3} = 3.888 \qquad c \approx 44.1\,fF$

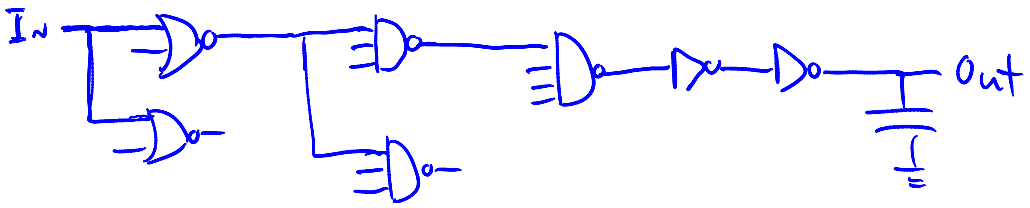
$\frac{c}{b} \cdot 2 = 3.888 \qquad b \approx 22.69\,fF$

$\frac{b}{a} = 3.888 \qquad a \approx 5.84\,fF$

Size	Value (fF)
a	5.84
b	22.69
c	44.1
d	102.88

d) **(4 pts)** By changing only the order (but not the types) of the gates, can you reduce the total capacitance of the gates in this chain? If so, draw the re-ordered chain (you do not need to recalculate the sizes) and explain why the capacitance is reduced; if not, explain why this isn't possible.

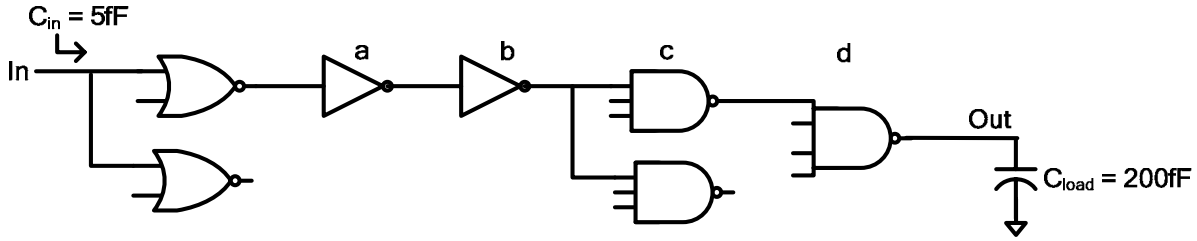
Yes - move the complex gates earlier into the chain:



The complex gates aren't very good drivers, so for the same EF they need to be substantially larger than an inverter. By moving the complex gates earlier, their capacitance is reduced by quite a bit more than the cap. of the inverters (which are moved closer to the final load) increases.

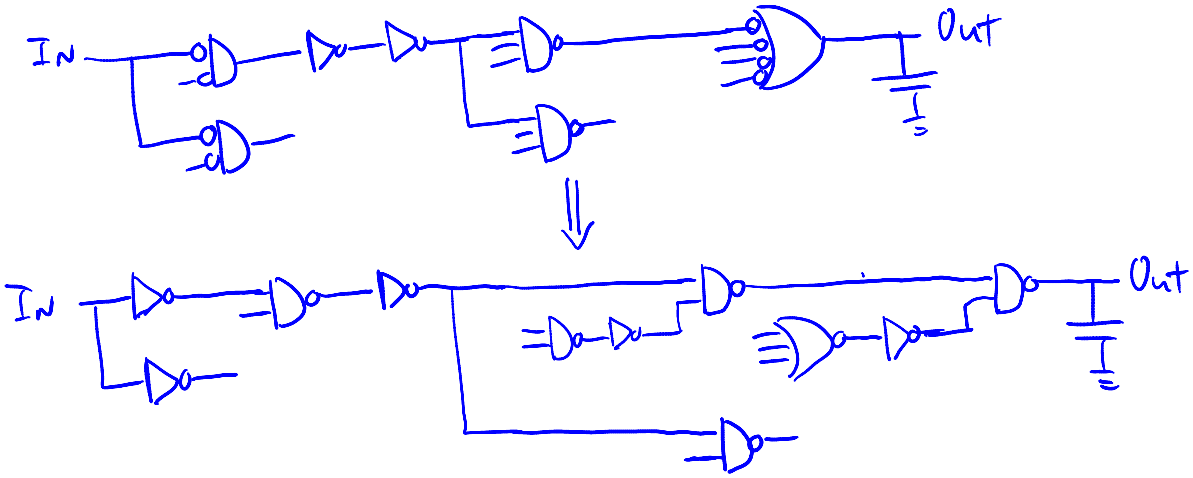
e) **(6 points)** While maintaining the same logical functionality and without changing C_{in}, can you improve the delay of this chain of gates (repeated below) by changing the number and/or types of gates? Please draw an improved schematic for the new chain of gates; you don't need to provide gate sizes.

Original chain:



Improved chain:

Since EF/stage is already close 4, don't really need to change # of stages - best bet is to reduce LE by moving logic off path and reducing gate complexity. Can also change NOR to NAND. Any logically equivalent solution with reduced LE will receive full credit; one possibility (and the transformations used to reach it) is shown below.



 $\Pi LE = (4/3)^3 = 2.37$