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Tuesday, October 6, 2009
6:30-8:00pm

EECS 141: FALL 2009—MIDTERM 1

For all problems, you can assume that all transistors have a channel length of 90nm and the following parameters (unless otherwise mentioned):

NMOS:
V_{Tn} = 0.2V, μ_n = 400 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, $\lambda = 0$
PMOS:
$|V_{Tp}|$ = 0.2V, μ_p = 200 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, $\lambda = 0$

NAME	Last First

GRAD/UNDERGRAD	

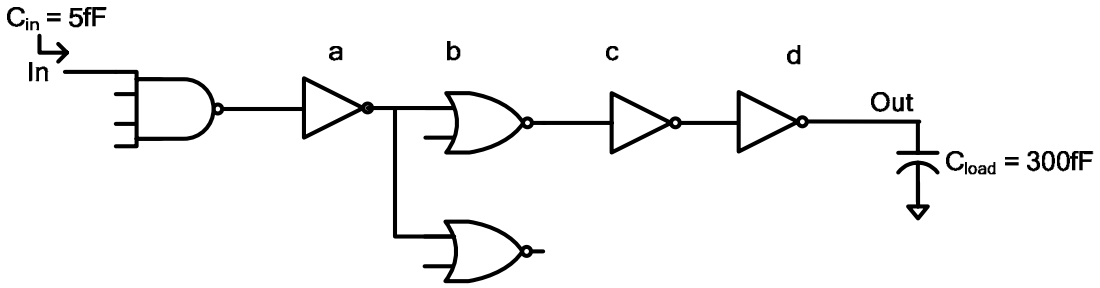
Problem 1: _____/ 30

Problem 2: _____/ 20

Problem 3: _____/ 20

Total: _____/ 70

PROBLEM 1. Logical Effort and Gate Sizing (30 points)



a) **(6 pts)** What is the path effort from In to Out?

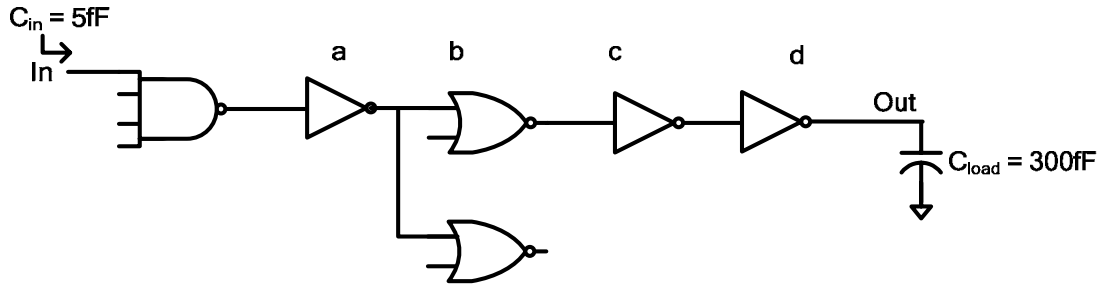
b) **(2 pts)** What EF/stage minimizes the delay of this chain of gates?

c) **(8 pts)** Size the gates to minimize the delay from In to Out.

Size	Value (fF)
a	
b	
c	
d	

d) **(6 pts)** While maintaining the same logical functionality and without changing C_{in}, can you improve the delay of this chain of gates (repeated below) by changing the number and/or types of gates? Please draw an improved schematic for the new chain of gates; you don't need to provide gate sizes.

Original chain:



Improved chain:

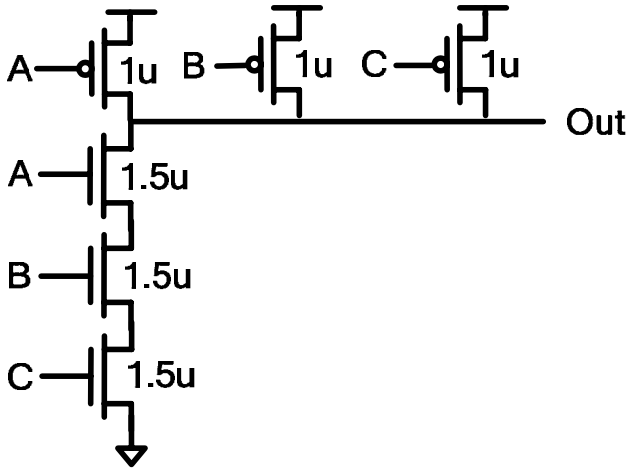
e) **(8 pts)** Now let's imagine that you are working in a new technology where the γ ($= C_D/C_G$) of the transistors is 100. Now how would you redesign the chain of gates in order to improve its delay? Please draw an improved schematic for the new chain of gates; you don't need to provide gate sizes. (You will receive partial credit if you can explain in general how γ should affect the design of the chain.)

PROBLEM 2. (20 pts) Complex Gates and Delay.

a) **(4 pts)** Implement the function $F = \overline{\left(\left(A \cdot B\right) + C\right) \cdot D}$ with a complex static CMOS gate.

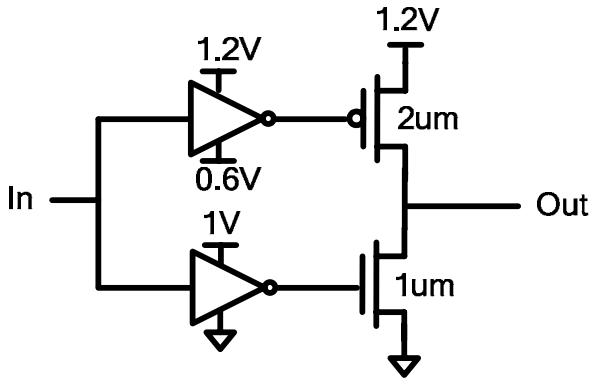
b) **(4 pts)** Assuming $R_{sqp} = R_{sqn}$, size your gate so that the worst-case pull up resistance is equal to the worst-case pull-down resistance. What is the logical effort of this gate from the A input?

c) **(12 pts)** Using the switch model for the transistors, what is the worst-case delay of the gate shown below? You can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10k\Omega/\square$, and $R_{sqp} = 20k\Omega/\square$, and you should provide your answer in ps.

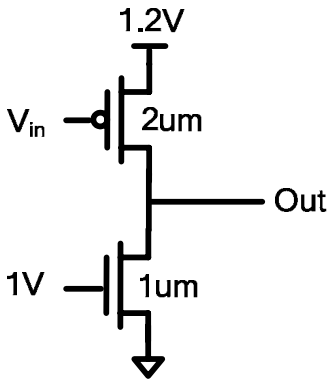


PROBLEM 3. (20 pts) Miscellaneous

a) **(8 pts)** Using the simple switch model of the transistors with R_{sqn} = 10kΩ/□, R_{sqp} = 20kΩ/□, and $V_{TN} = |V_{TP}| = 0.2V$, draw the VTC of the circuit shown below and provide the values of V_{OH}, V_{OL}, V_{IH}, and V_{IL}. You can assume that the NMOS and PMOS transistors inside of the inverters are sized such that their on-resistances are equal.



b) **(6 pts)** Using the velocity saturated model and assuming that both of the transistors below operate in saturation, what value of V_{in} makes the drain current of the two transistors equal to each other?..



c) (**6 points)** How much total energy is dissipated by the inverter shown below when In steps from 1.2V to 0V and then back to 1.2V? You can ignore all capacitors associated with the transistors inside of the inverter.