**University of California**
**College of Engineering**
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**Tuesday, October 6, 2009**
**6:30-8:00pm**

# EECS 141: FALL 2009—MIDTERM 1

**For all problems, you can assume that all transistors have a channel length of 90nm and the following parameters (unless otherwise mentioned):**

**NMOS:**
$V_{Tn}$ = 0.2V, $\mu_n$ = 400 cm$^2$/(V·s), $C_{ox}$ = 1.125 μF/cm$^2$, $v_{sat}$ = 1e7 cm/s, λ = 0
**PMOS:**
$|V_{Tp}|$ = 0.2V, $\mu_p$ = 200 cm$^2$/(V·s), $C_{ox}$ = 1.125 μF/cm$^2$, $v_{sat}$ = 1e7 cm/s, λ = 0

| **NAME** | Last Solutions First |
|---|---|

| **GRAD/UNDERGRAD** | |
|---|---|

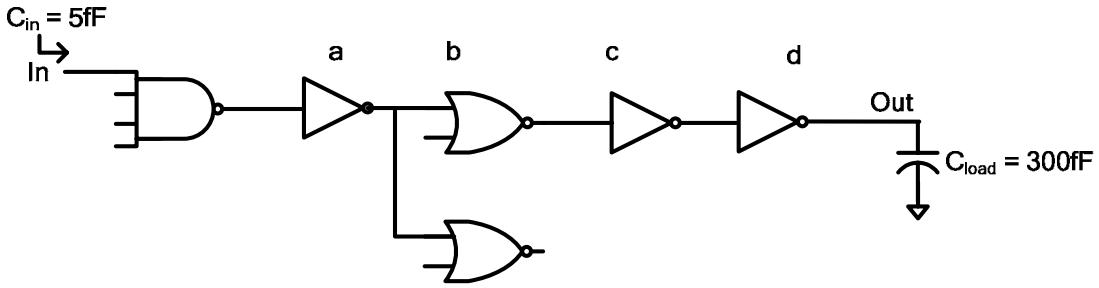
**Problem 1: _____/ 30**

**Problem 2: _____/ 20**

**Problem 3: _____/ 20**

**Total: _____/ 70**

**PROBLEM 1. Logical Effort and Gate Sizing (30 points)**




a) **(6 pts)** What is the path effort from In to Out?

$F = 300ff/5ff = 60$

$\Pi LE = 2 \cdot 5/3 = 10/3$

$\Pi B = 2$

$PE = F \cdot \Pi LE \cdot \Pi B$

$\boxed{PE = 400}$

b) **(2 pts)** What EF/stage minimizes the delay of this chain of gates?

$EF_{opt} = \sqrt[5]{PE}$

$\boxed{EF_{opt} \approx 3.31}$

c) **(8 pts)** Size the gates to minimize the delay from In to Out.

$d = \frac{300ff}{3.31} \approx 90.63\,ff$

$c = \frac{d}{3.31} \approx 27.38\,ff$

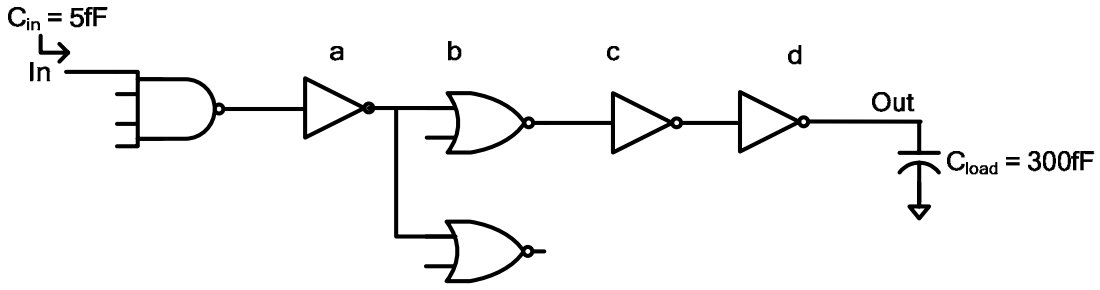
$b = \frac{5}{3} \cdot \frac{c}{3.31} \approx 13.79\,ff$

$a = 2 \cdot \frac{b}{3.31} \approx 8.33\,ff$

| Size | Value (fF) |
|---|---|
| a | 8.33 |
| b | 13.79 |
| c | 27.38 |
| d | 90.63 |

d) **(6 pts)** While maintaining the same logical functionality and without changing $C_{in}$, can you improve the delay of this chain of gates (repeated below) by changing the number and/or types of gates? Please draw an improved schematic for the new chain of gates; you don't need to provide gate sizes.

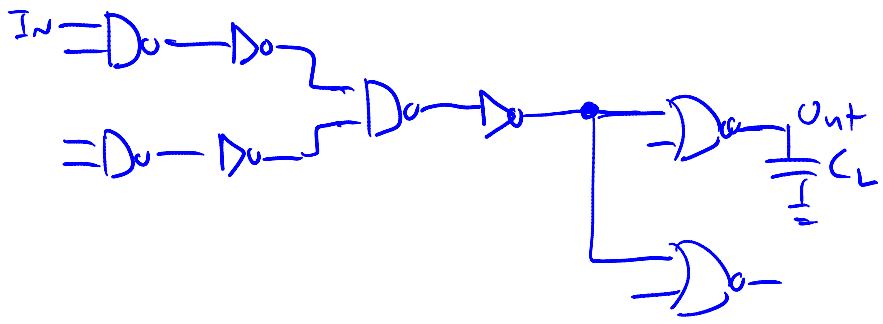
Original chain:




Improved chain:

Optimal number of stages: $\log_4(400) \approx 4.32$

So, 5 stages is about right. However, we have a 4-input NAND (which has large LE) at the beginning of the chain, and we also have a bunch of inverters. So, in order to reduce the LE, we can replace the 4-input gate with a cascade of 2-input gates and inverters:



e) **(8 pts)** Now let's imagine that you are working in a new technology where the γ (= $C_D/C_G$) of the transistors is 100. Now how would you redesign the chain of gates in order to improve its delay? Please draw an improved schematic for the new chain of gates; you don't need to provide gate sizes. (You will receive partial credit if you can explain in general how γ should affect the design of the chain.)

Remember that delay optimal $f$ (and equivalently, EF) is set only by $\gamma$:

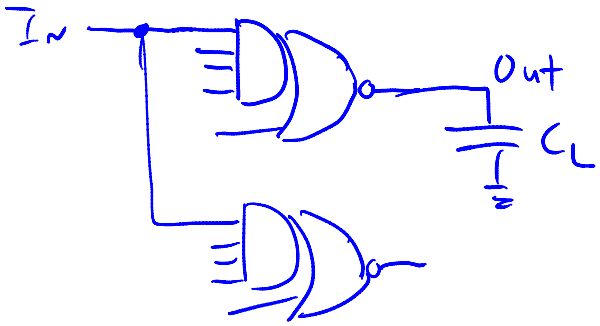
$$f = e^{(1+\gamma/f)}$$

$$\gamma = 100 \longrightarrow f \approx 37.9$$

In other words, with such a large $\gamma$, the optimal fanout is also substantially larger than 4. Therefore, the optimal number of stages will be much smaller:

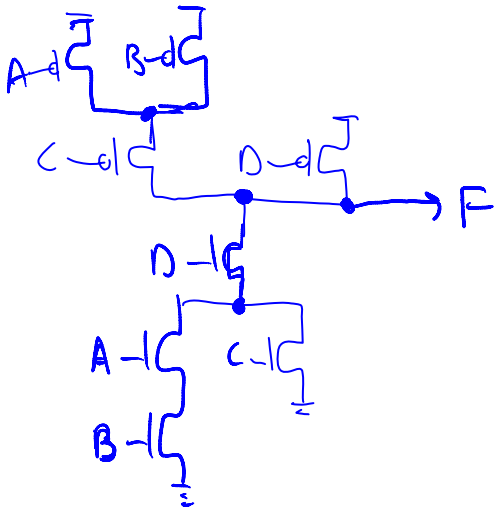
$$N_{opt} = \log_{37.9}(PE) \approx 1.65$$

To get the logical polarity right, this would lead us to a 1 stage implementation:

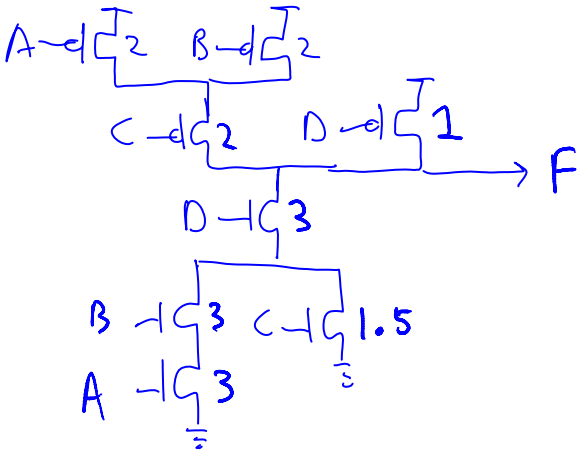


**PROBLEM 2. (20 pts) Complex Gates and Delay.**

a) **(4 pts)** Implement the function $F = \overline{((A \cdot B) + C) \cdot D}$ with a complex static CMOS gate.




b) **(4 pts)** Assuming $R_{sqp} = R_{sqn}$, size your gate so that the worst-case pull up resistance is equal to the worst-case pull-down resistance. What is the logical effort of this gate from the A input?

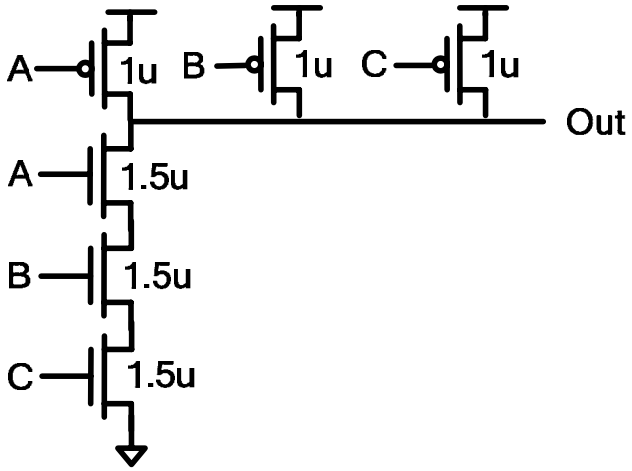



$LE_A = \frac{C_{in,A}}{C_{in,inv}}$

$LE_A = \frac{5}{2}$

Reference inverter: 1 / 1 / 2

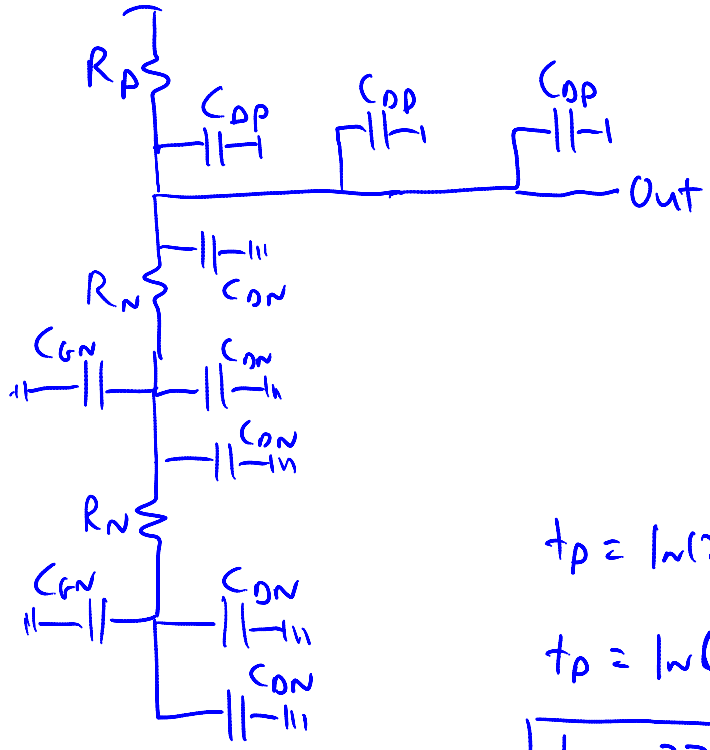
c) **(12 pts)** Using the switch model for the transistors, what is the worst-case delay of the gate shown below? You can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10k\Omega/\square$, and $R_{sqp} = 20k\Omega/\square$, and you should provide your answer in ps.




The first thing to realize here is that the worst-case delay occurs when A=B=1 and C goes from 1 to 0.

(You can see this by noticing that in this case a single PMOS transistor has to drive all of the internal caps of the stack.)

RC model:




$$R_p = 20k\Omega/\square \cdot \frac{90nm}{1\mu m} = 1.8k\Omega$$

$$R_N = 10k\Omega/\square \cdot \frac{90nm}{1.5\mu m} = 600\Omega$$

$$C_{DP} = 2fF/\mu m \cdot 1\mu m = 2ff$$

$$C_{DN} = 2fF/\mu m \cdot 1.5\mu m = 3ff$$

$$C_{GN} = C_{DN} = 3ff$$

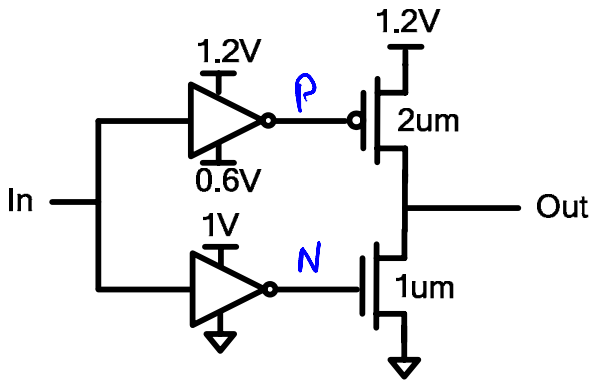
$$t_p = \ln(2) \cdot R_p \cdot (3C_{DP} + 5C_{DN} + 2C_{GN})$$

$$t_p = \ln(2) \cdot 1.8k\Omega \cdot (6ff + 15ff + 6ff)$$

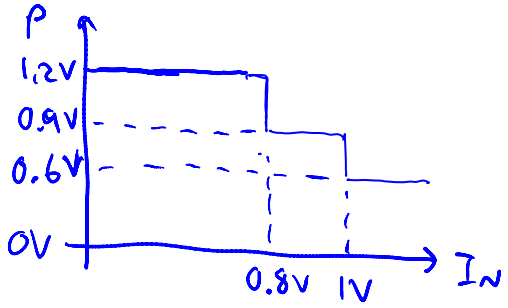
$$\boxed{t_p \approx 33.7ps}$$

**PROBLEM 3. (20 pts) Miscellaneous**

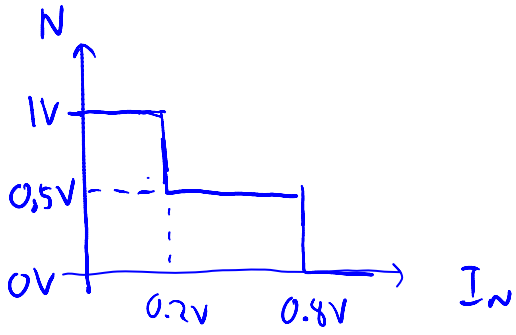
a) **(8 pts)** Using the simple switch model of the transistors with $R_{sqn}$ = 10kΩ/□, $R_{sqp}$ = 20kΩ/□, and $V_{TN} = |V_{TP}| = 0.2V$, draw the VTC of the circuit shown below and provide the values of $V_{OH}$, $V_{OL}$, $V_{IH}$, and $V_{IL}$. You can assume that the NMOS and PMOS transistors inside of the inverters are sized such that their on-resistances are equal.



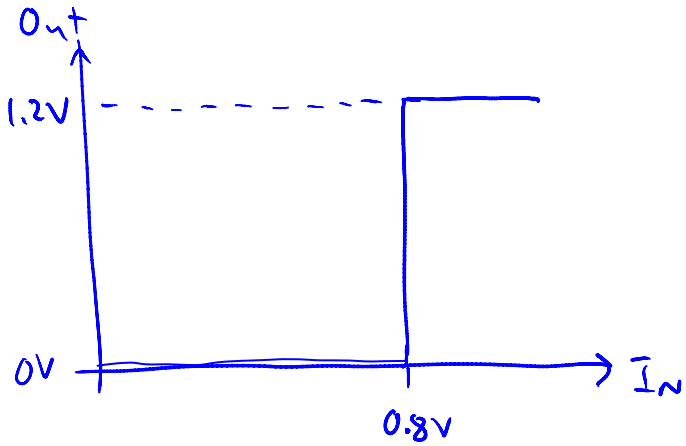

VTC of P:




VTC of N:




VTC from In to Out:



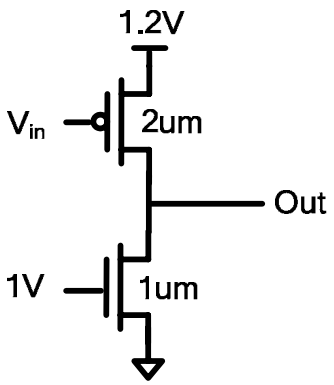

$V_{OH} = 1.2V$

$V_{OL} = 0V$

$V_{IH} = 0.8V$

$V_{IL} = 0.8V$

b) **(6 pts)** Using the velocity saturated model and assuming that both of the transistors below operate in saturation, what value of $V_{in}$ makes the drain current of the two transistors equal to each other?.




$$\xi_{cn} = \frac{2v_{sat}}{\mu_n} = \frac{2e7\ cm/s}{400\ cm^2/Vs} = 5MV/m$$

$$\xi_{cp} = \frac{2v_{sat}}{\mu_p} = \frac{2e7\ cm/s}{200\ cm^2/Vs} = 10MV/m$$

$$I_{Dp} = W_p v_{sat_p} C_{ox_p} \frac{(1.2V - V_{in} - |V_{Tp}|)^2}{1.2V - V_{in} - |V_{Tp}| + \xi_{cp} \cdot L} \qquad \xi_{cp} L = 0.9V$$

$$I_{Dn} = W_n v_{sat_n} C_{ox_n} \frac{(1V - V_{Tn})^2}{1V - V_{Tn} + \xi_{cn} L} \qquad \xi_n L = 0.45V$$

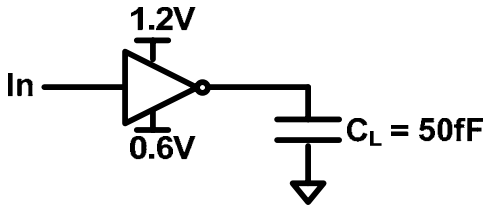
$$I_{Dp} = I_{Dn} \rightarrow I_{Dp}/I_{Dn} = 1$$

$$\frac{I_{Dp}}{I_{Dn}} = \frac{2\mu m}{1\mu m} \cdot \frac{(1V - V_{in})^2 \,/\!/\, (1V - V_{in} + 0.9V)}{(0.8V)^2 / (0.8V + 0.45V)} = 1$$

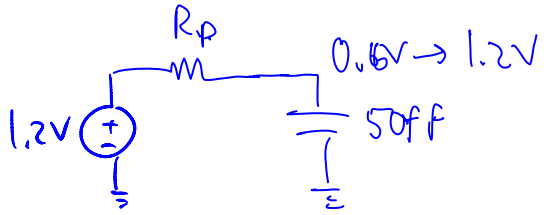
$$(1V - V_{in})^2 = 0.256V \cdot (1.9V - V_{in})$$

$$\hookrightarrow \boxed{V_{in} \approx 375mV}$$

c) **(6 points)** How much total energy is dissipated by the inverter shown below when In steps from 1.2V to 0V and then back to 1.2V? You can ignore all capacitors associated with the transistors inside of the inverter.



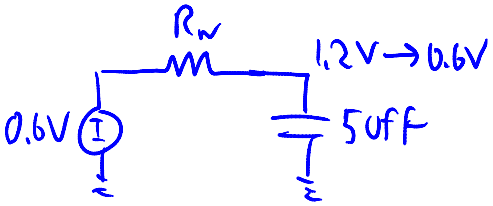

$I_N$: 1.2V → 0V:




$Q = (1.2V - 0.6V) \cdot 50fF = 30fC$

$E_{1.2V} = Q \cdot 1.2V = 36fJ$

$I_N$: 0V → 1.2V:




$Q = (0.6V - 1.2V) \cdot 50fF = -30fC$

$E_{0.6V} = Q \cdot 0.6V = -18fJ$

(Charge flows in to 0.6V supply, so energy is indeed returned to that supply.)

$E_{inverter} = E_{1.2V} + E_{0.6V}$

$E_{inverter} = 18fJ$