

Problem 1: Power (12pts)

Consider the circuit of Fig. 1. The signal waveforms of each signal within one period are shown in Fig. 2. You may assume that these signals are repeated with a frequency of 1MHz (or $T = 1 \mu s$). Use the following device parameters: $V_T = 1/2V$; $\gamma = 0$; $R_{on} = 10 \text{ k}\Omega$, $R_{off} = \text{infinity}$. You may ignore the parasitic capacitances of the transistors.

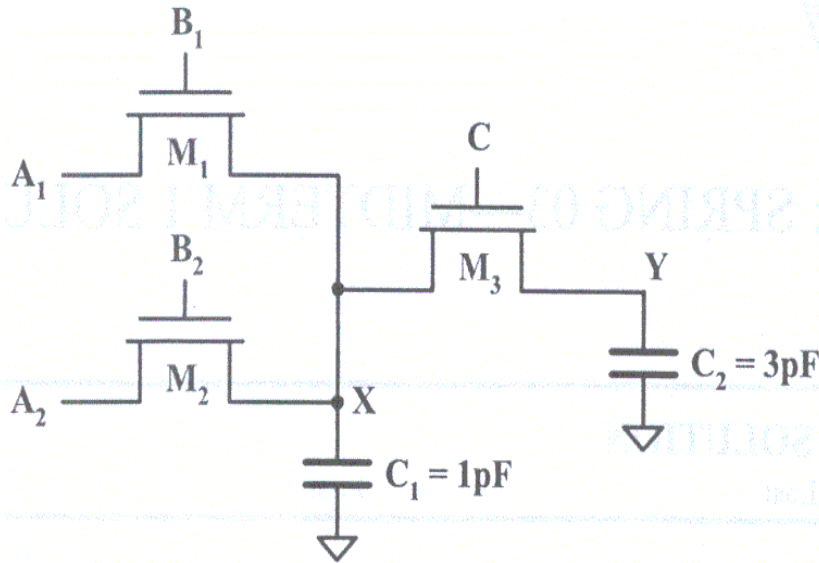


Fig. 1

a. Draw the waveform of the signals on nodes X and Y, assuming that all input signals are switching between 0 and 2V (4 pts)

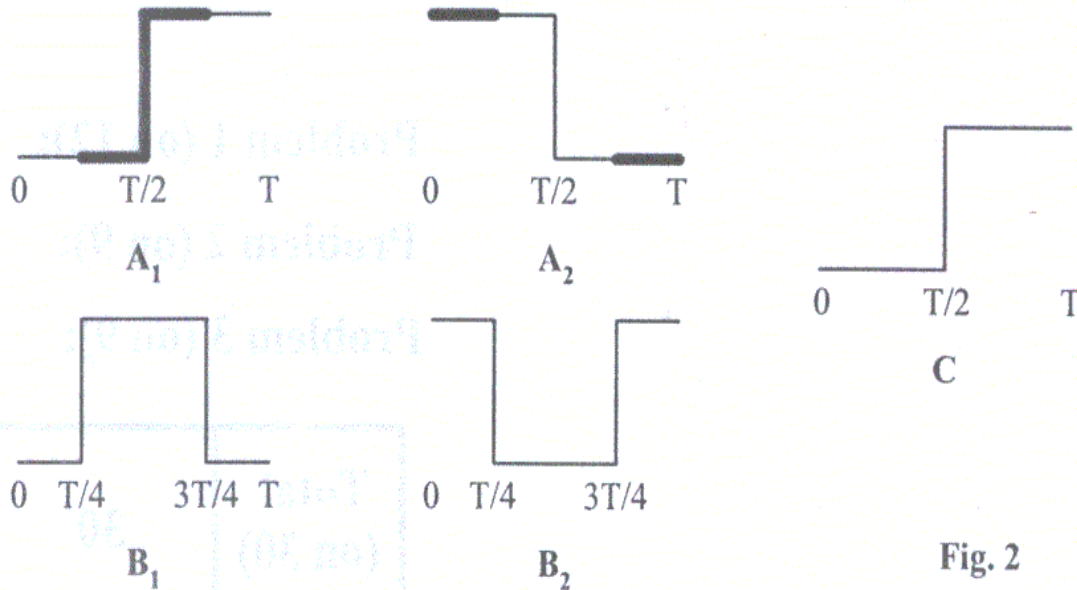
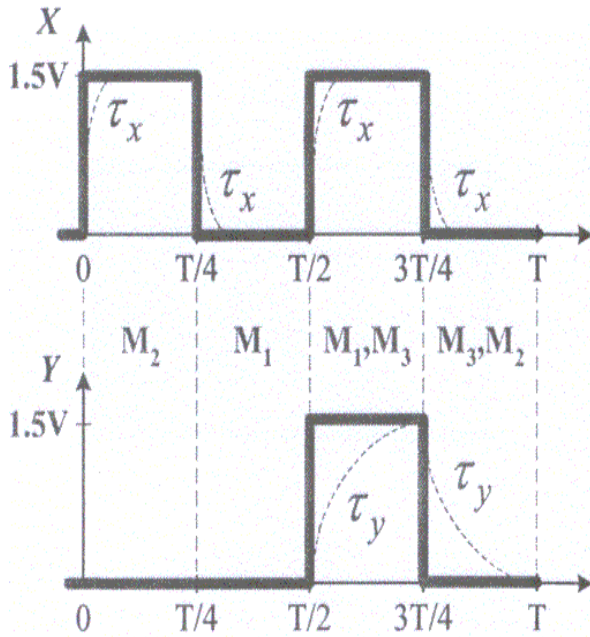


Fig. 2



Signals of nodes X and Y reach $V_{DD} - V_T = 1.5V$.

Conducting devices are labeled in the graph.

Full credit for square waveforms on the left!

Extra points if you considered time constants as indicated by thin lines. ($T/4 = 250ns$).

$$\tau(x) = R_{on} * V_{DD} = 10ns$$

$$\tau(y) = R_{on}C_1 + (R_{on}+R_{on})C_3 = 70ns$$

Resulting waveforms are shown above.

b. Calculate the dynamic power dissipation on this circuit (2pts)

$$P_{dyn} = \alpha * f * C * V_{DD} * (V_{DD} * V_T)$$

Signal at node X makes two transitions during one clock period, so the energy per transition at node X has to be doubled. The total dynamic power consumption is therefore given by:

$$P_{dyn} = f * (2C_1 + 2C_3) * V_{DD} * (V_{DD} - V_T) = 15\mu W$$

c. The power consumption of the CMOS inverter can be minimized through circuit optimizations. Determine how each circuit parameter mentioned in the table should be changed to reduce the different inverter power consumption components (6pts)

For each parameter, fill in one of the following choices in the blanks:

A - Increase

B - Decrease

C - Doesn't affect this type of power consumption

Goal	Circuit Parameter Optimization	A, B or C
Minimize the dynamic power consumption due to CL charging and discharging	Vdd	B
	CL	B
	Transistor abs(V_{th})	C

	Transistor widths (first order)	C
Minimize the direct-path power consumption (assume a fixed rise and fall time at the input)	Vdd	B
	CL	A
	Transistor abs(Vth)	A
	Transistor widths	B
Minimize the static power dissipation	Vdd	B
	CL	C
	Transistor abs(Vth)	A
	Transistor widths	B

Problem 2: VTC and propagation delay (9 pt)

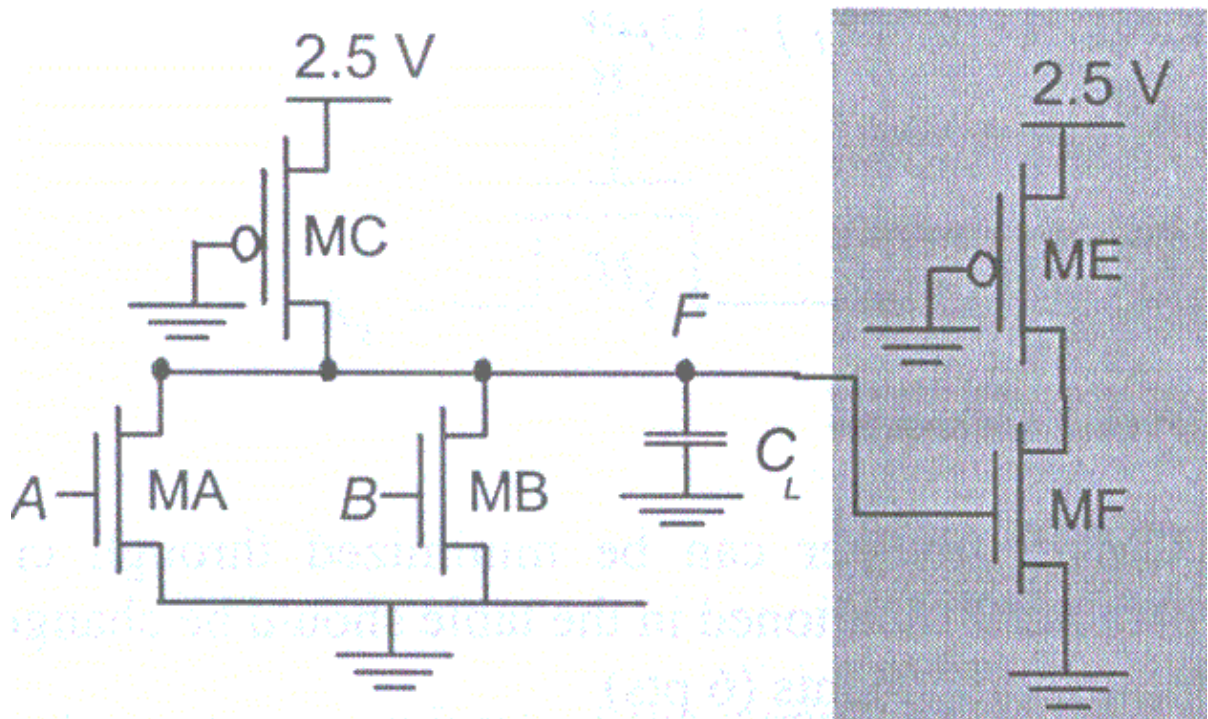
Consider the digital circuit shown below. It pictures an alternative 2-input NOR gate followed by a single fanout inverter.

To make the analysis of this circuit easy, we are using simplified transistor models.

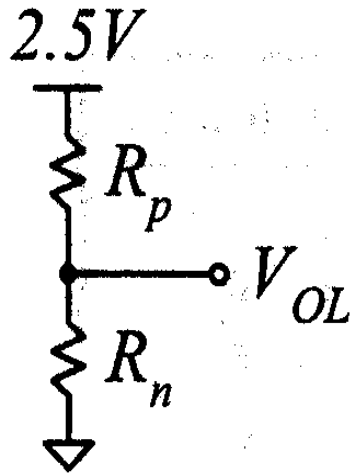
First of all, we assume that the transistor can be represented by a linear resistor, this is

NMOS (for $W/L = 1$): $R_{N_{on}} = 10 \text{ k}\Omega$; $R_{N_{off}} = \text{infinity}$; $V_{TN} = 0.75 \text{ V}$;

PMOS (for $W/L = 1$): $R_{P_{on}} = 20 \text{ k}\Omega$; $R_{P_{off}} = \text{infinity}$; $V_{TP} = -0.75 \text{ V}$;



- a. Assume that the PMOS is of minimum size (this is, $W/L = 1$). Determine the sizes of the two NMOS transistors MA and MB so that the V_{OL} of the NOR gate is at most 0.5V. Also describe under what conditions this happens (2pts)



$(W/L)_{MA} = 2$
 $(W/L)_{MB} = 2$

b. The parasitic capacitances of a unit size NMOS and PMOS transistors are given in the table below. You may assume that all capacitances are constant and linear over the operation range. Determine the equivalent load capacitance at the output of the NOR gate (i) for A switching from 0 to 1, and B=0; (ii) for A and B switching simultaneously from 0 to 1. You should use the sizes derived in a. for both the NOR gate and the fanout inverter (4pts)
 Hint: In the case you are not sure about your answer in a, use $(W/L)_{NMOS} = 3$

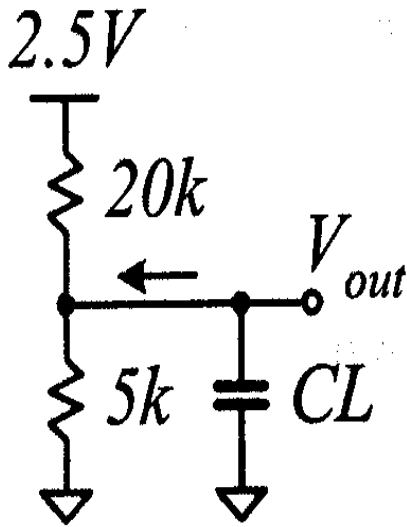
Cap in fF	C_{gs}	C_{gd}	C_{gb}	C_{sb}	C_{db}
NMOS	0.1	0.15	0.2	0.25	0.3
PMOS	0.12	0.17	0.22	0.27	0.32

Table below summarizes the contribution for each transistor (factor 2 is due to Miller effect):

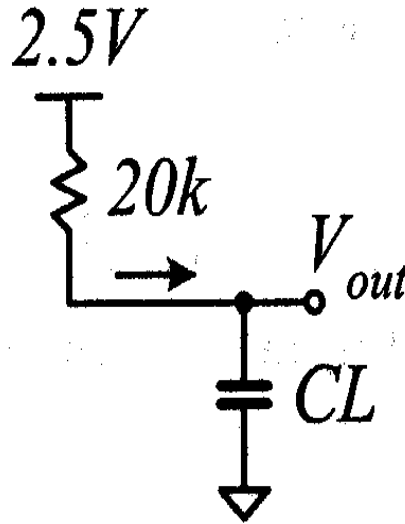
Transistor (size W/L)	(i) A: 0 to 1, B = 0	(ii) A, B: 0 to 1
MA(2)	$C_{db} + 2C_{gd}$	same
MB(2)	$C_{db} + C_{dg}$	$C_{db} + 2C_{gd}$
MC(1)	$C_{db} + C_{dg}$	same
MF(2)	$C_{gs} + C_{gb} + C_{gd}$	same
Total CL	3.49 fF	3.79 fF

For total C, you need to multiply numbers from Table 1 by (W/L) of each transistor

c. Determine the propagation delay of the NOR gate for A switching from 0 to 1 and 1 to 0, while B=0. For C_l use the answer you got in b. In not sure use, $C_l = 8fF$. You may assume that the V_M of the gate is approx at $V_{DD}/2$ (3pts)



A: 0 → 1, B=0



A: 1 → 0, B=0

A: 0 to 1, worst case longest delay occurs when only one NMOS is "on"

$$t(p0 \text{ to } 1) = 0.69 CL * (20k \parallel 5k)$$

A: 1 to 0

$$t(p1 \text{ to } 0) = 0.69 * CL * 20k = 52.30 \text{ ps}$$

Acceptable answers

$$t(p0 \text{ to } 1) = 6.6\text{ps (also OK: 9.4ps)}$$

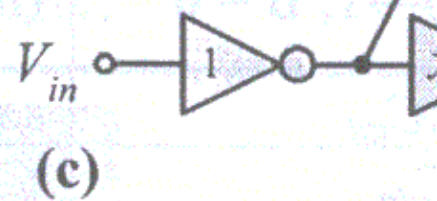
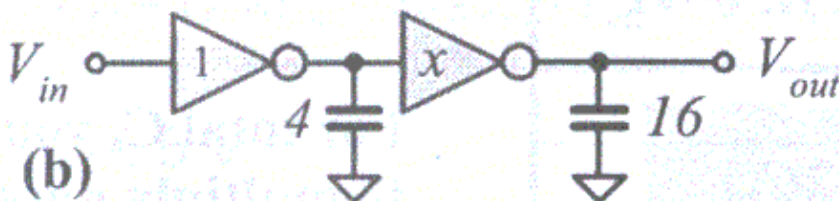
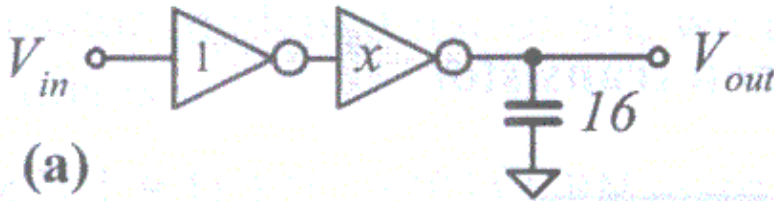
$$t(p1 \text{ to } 0) = 48.3 \text{ ps}$$

$$CL = 8\text{fF} = 15.0 \text{ ps (also OK: 22,1 ps)}$$

$$CL = 8\text{fF} - 110.4\text{ps}$$

Problem 3: Sizing (9pts)

The circuits shown in the figure below illustrate the impact of small topological changes on the delay and energy, when driving a fixed load at the output. You may assume $\gamma = 1$ (or $C_{intrinsic} = C_{gate}$). For each of the circuits in the Figure, calculate the following:



a. Size x of the second inverter in the chain to minimize propagation delay from the input V_{in} to output V_{out} (6pts)

Hint: do not blindly use the equations given in the book.

Gate delay is given by:

$$t_p = t_{p0} * (1 + f/y)$$

Using this equation we can obtain total delay as follows:

(a) delay total = $(1 + x/1) + (1 + 16/x) \Rightarrow x = 4$

note: this is well-known geometric mean result

(b) delay total = $(1 + (4+x)/1) + (1 + 16/x) \Rightarrow x = 4$

note: geometric mean result ($x=2.5$) is wrong in this case! For exercise plug in $x = 2.5$ and $x = 4$ in the delay formula and check which result gives smaller delay.

(c) delay total = $(1 + (4+x)/1) + (1 + 16/x) \Rightarrow x = 2$

note: geometric mean result is valid again (no fixed side-loads)

b. Energy consumed by the shaded path in all three cases (3pts). You may assume that $V_{DD} = 1V$, and the capacitances are given in fF. (3pts).

Total energy of the gate can be simply obtained with following formula:

$$E = (C_{intrinsic} + C_{gate}) * V_{DD}^2$$

Using this result, simply plug in the numbers from (a):

$$E(a) = [(1+x) + (x+16)] * V_{DD}^2 = 24fJ$$

$$E(b) = [(1+x+4) + (x+16)] * V_{DD}^2 = 29fJ$$

$$E(c) = [(1+4x) + (x+16)] * V_{DD}^2 = 27fJ$$

Note: although not correct, it is also acceptable if you included C_{in} of the first stage. (+ 1fJ to these numbers)