Department of Electrical Engineering and Computer Sciences
College of Engineering
University of California, Berkeley

SR Sanders Spring 2002

EECS40 - Midterm #2
April 11, 2002

Name: _____ **SID#** _____
Last, First

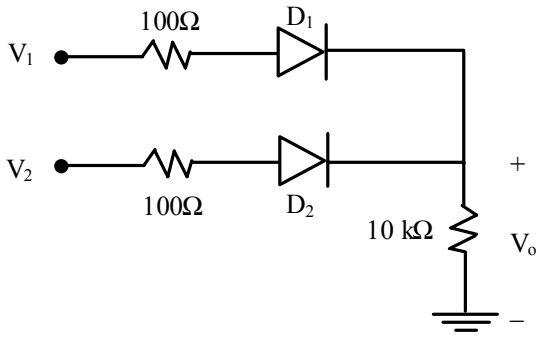
Signature: _____ **TA**: David ☐
Richard ☐
Frank ☐

Guidelines

1. Closed book, except 2 sheets of your own notes.
2. You may use a calculator.
3. Do not unstaple the exam.
4. Show all your work and reasoning on the exam to receive full or partial credit.
5. The exam has 4 problems.

Problem	Points possible	Your score
1	**20**	
2	**20**	
3	**30**	
4	**30**	
total		

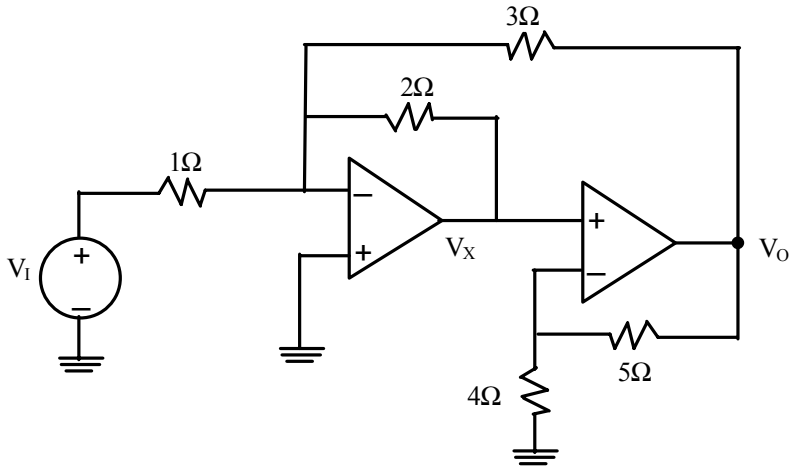
(20) 1. Consider the diode logic (DL) circuit shown below. Fill in the table below. What logic operation does the circuit perform? Assume the diodes are perfect rectifiers and that logic low is 0-1V and logic high is 4-5V. You must show all your work.



V_1	V_2	V_O
0V (0)	0V (0)	
0V (0)	5V (1)	
5V (1)	0V (0)	
5V (1)	5V (1)	

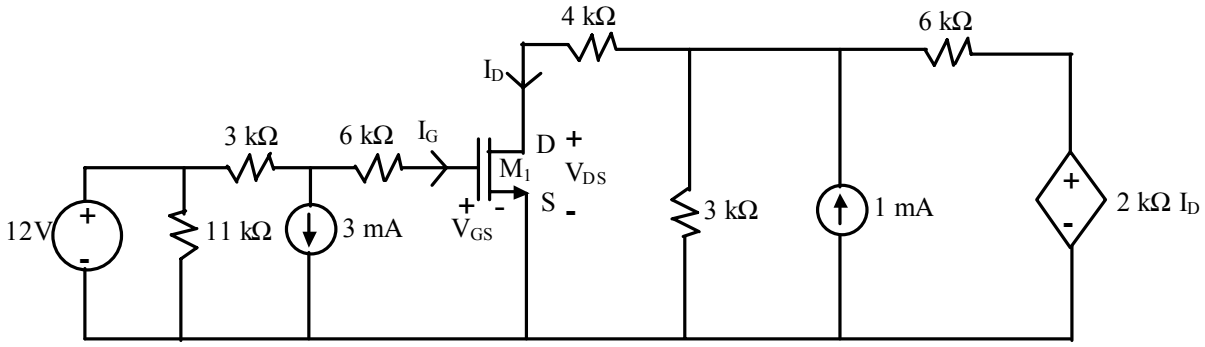
Logic operation:

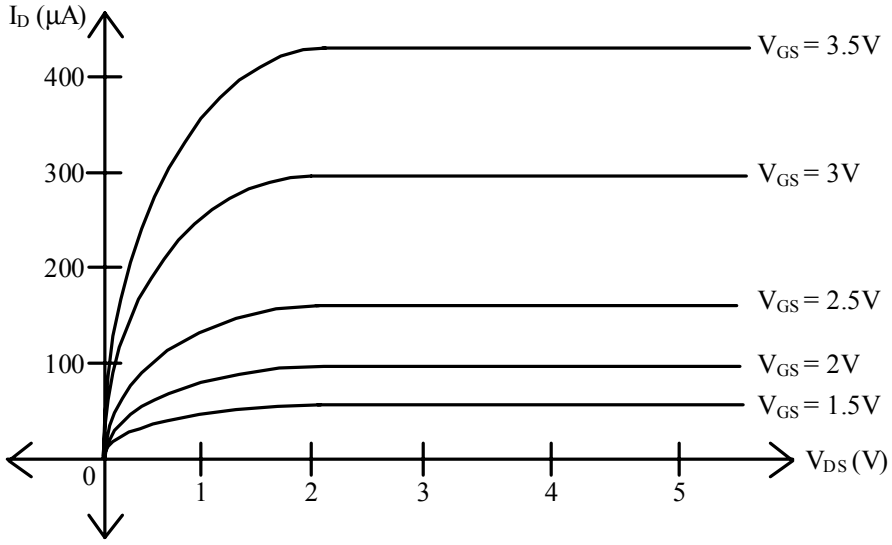
(20) 2. Consider the circuit shown below. Find V_o as a function of V_i and put your answer in the box below.



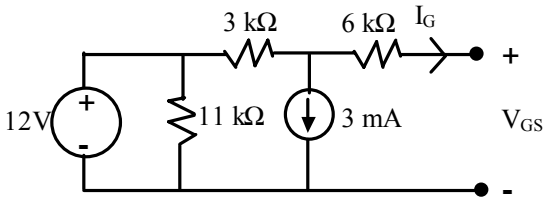
V_o =

(30) 3. Consider the circuit and IV curve for M1 shown below





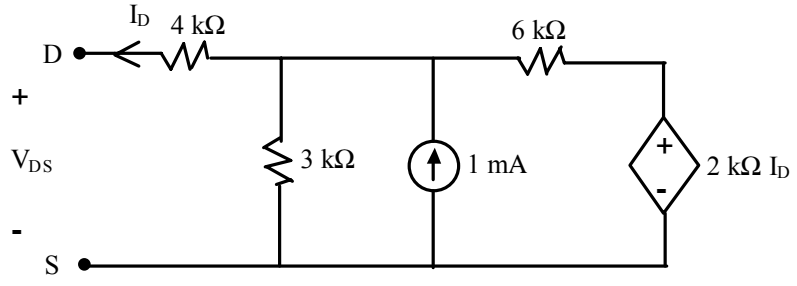
(6) a) Thevenize the left hand side of the circuit and put your answer in the box provided below (6 pts).



V_{th}=	R_{th}=

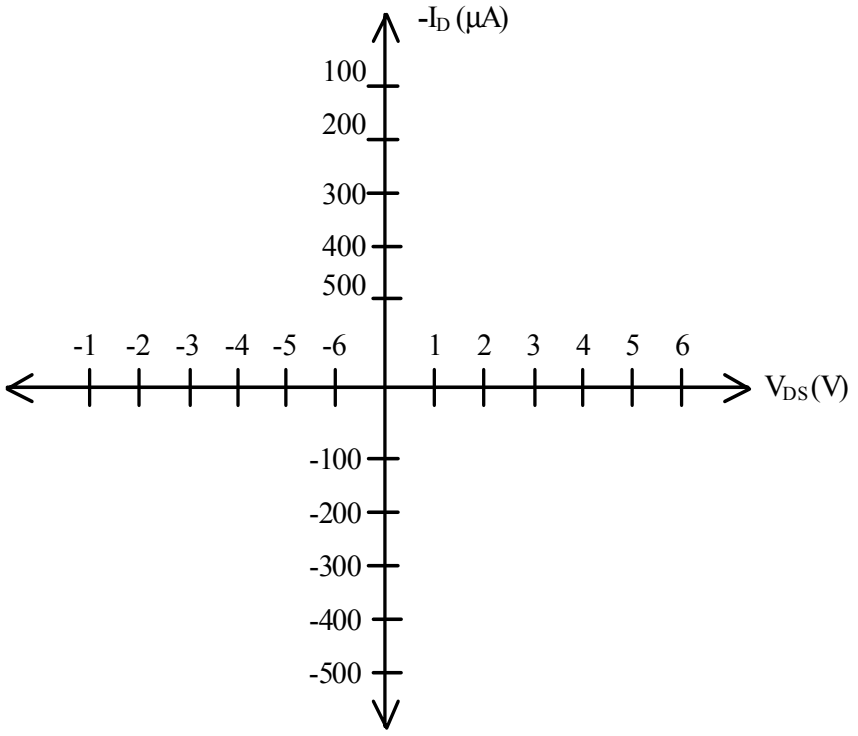
(12) b) Thevenize the right hand side of the circuit and put your answer in the box provided below (8 pts).

Draw the Thevenin equivalent circuit and the corresponding IV curve ($-I_D$ versus V_{DS}) (4 pts). Note: We WILL cascade your errors from the Thevenin equivalent.



V_{th}=	R_{th}=

Thevenin Equivalent Circuit:



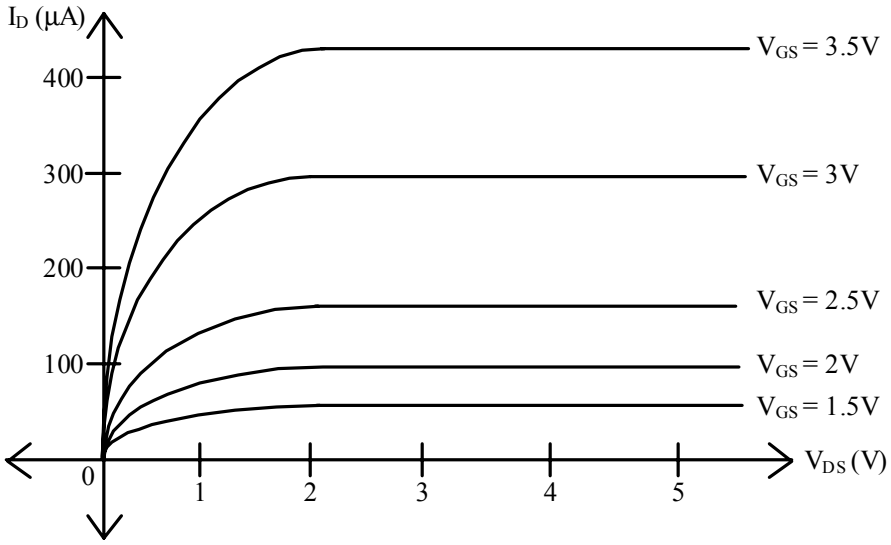
(6) c) What is the operating point of the MOSFET M1 (6 pts)? Put your answer in the box below. If you were unable to obtain answers for part a) and/or part b), then use the values shown below. Of course the values may or may not be correct:

part a) $V_{th} = 2V$
$R_{th} = 2k\Omega$

part b) $V_{th} = 4V$
$R_{th} = 10k\Omega$

Note: We will NOT cascade your errors or take off points for using the above values.

MOSFET M1 IV Curve



V_{DS}=	I_D=

(6) d) How much power does the MOSFET M1 absorb (6 pts)? Put your answer in the box provided below. If you were unable to obtain answers for part a), part b), and/or part c), then use the values shown below. Of course the values may or may not be correct.

part a) $V_{th} = 2V$
$R_{th} = 2k\Omega$

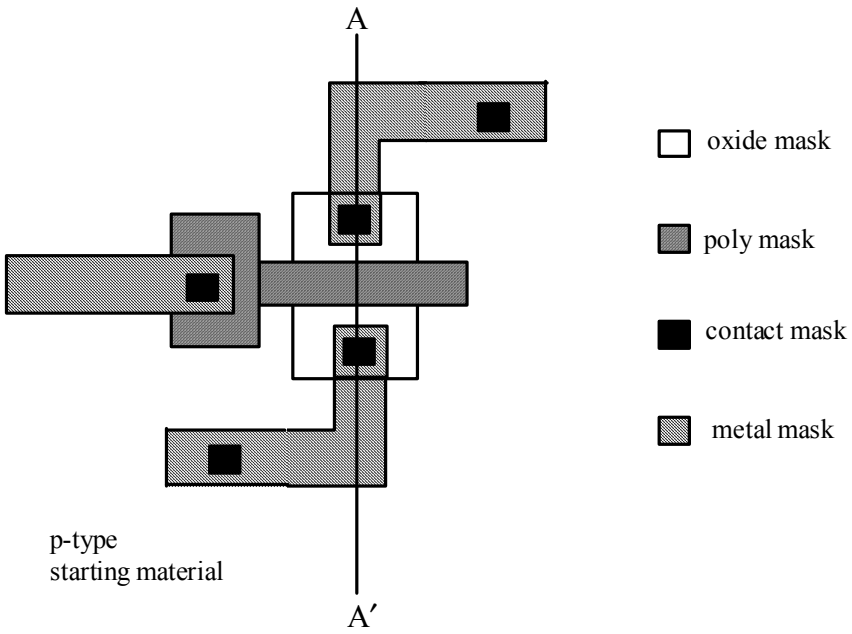
part b) $V_{th} = 4V$
$R_{th} = 10k\Omega$

part c) $V_{DS} = 2V$
$I_D = 200\,\mu A$

Note: We will NOT cascade your errors or take off points for using the above values.

$P_{absorbed/M1} =$

(30) 4. Given the mask layout for an NMOS transistor shown below, give the process steps (i.e. recipe) to create an NMOS transistor. We are giving you a lot of freedom in regards to poly thickness, oxide thickness, and drain/source depths. However, be realistic: for example, do not grow 500nm of gate oxide.



Hint: If you are stuck and think Prof. Sanders and the TAs are evil, try drawing the final cross-section of A-A′ and walk yourself step-by-step through the process.

Process Steps

1)