University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 Midterm II

Spring 1999 Prof. Roger T. Howe April 14, 1999

Name: _____ ***Student ID*** _____
last, first

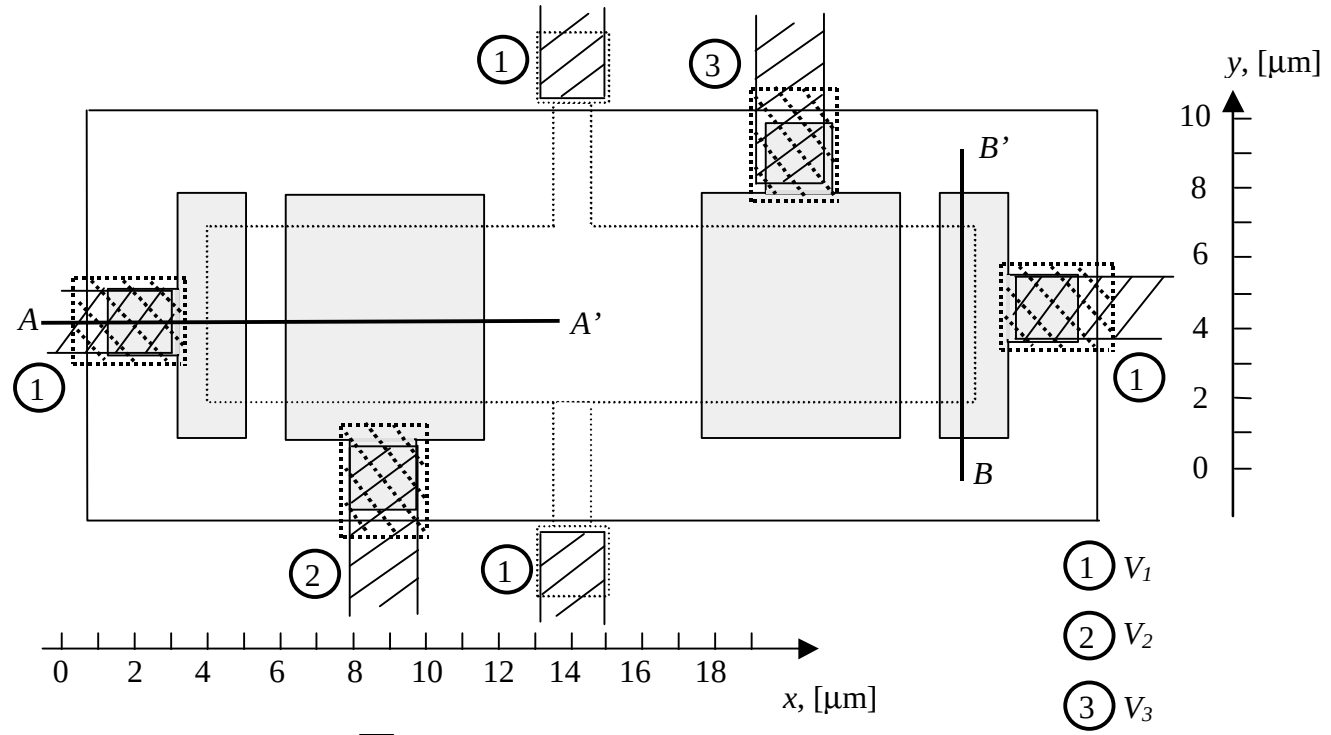
Guidelines

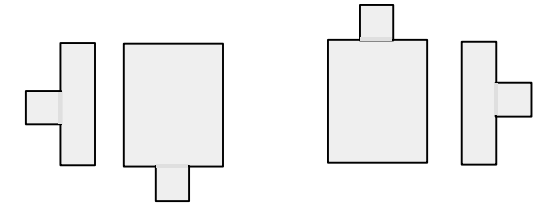
1. Closed book and notes; one 8.5" x 11" page (both sides) of your own notes is allowed.
2. You may use a calculator.
3. Do not unstaple the exam.
4. Show *all your work and reasoning on the exam* in order to receive full or partial credit.

Score

Problem	Points Possible	Score
1	20	
2	20	
3	10	
Total	50	

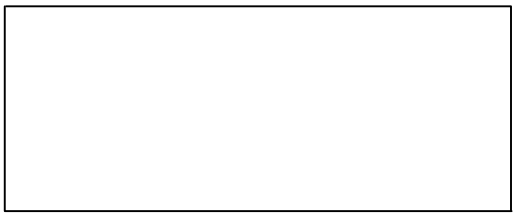
1. Micromirror Structure [20 points]





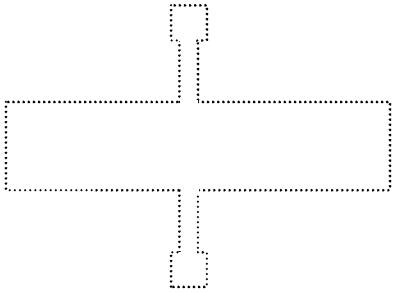
Poly1 Mask
(clear field)

Oxide2 Mask
(dark field)



Oxide1 Mask
(clear field)

Metal Mask
(clear field)



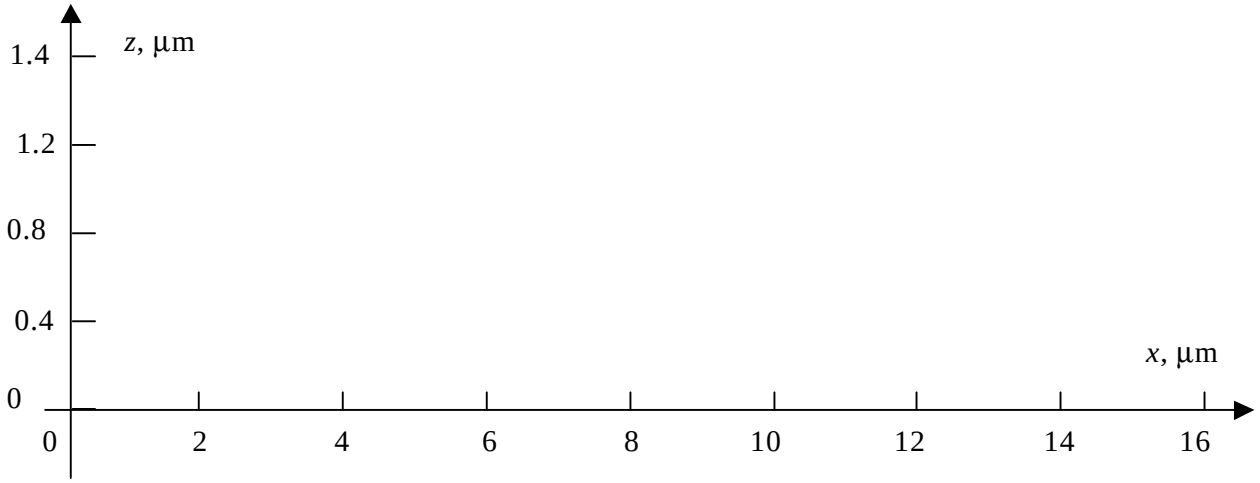
Poly2 Mask
(clear field)

Process Sequence:

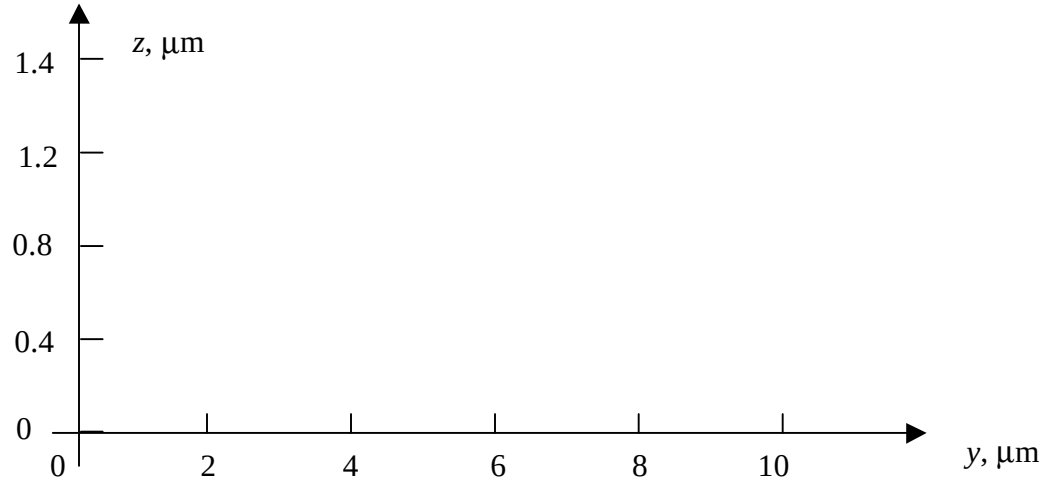
1. Starting material: phosphorus-doped silicon, concentration 5 x 10^{16} cm^{-3}
2. Deposit 200 nm of silicon nitride (see properties below)
3. Deposit 200 nm of n-type polysilicon and pattern using **poly1 mask** (clear field)
4. Deposit 400 nm of silicon dioxide and pattern using the **oxide1 mask** (clear field).
5. Deposit 250 nm of n-type polysilicon and pattern using the **poly2 mask** (clear field)
6. Spin photoresist, expose with the **oxide2 mask** (dark field), develop, and etch 400 nm of oxide, strip photoresist.
7. Deposit 250 nm of gold and pattern using the **metal mask** (clear field)
8. Etch in hydrofluoric acid long enough to remove all remaining oxide; rinse, and dry.

Silicon nitride: $\varepsilon_n = 7.5\ \varepsilon_o$ where εo is the permittivity of air or vacuum (8.85 x 10^{-14} F/cm). It is not etched in any of the processes used to etch oxide, polysilicon, or gold.

(a) [7 pts.] Sketch the cross section ***A-A'*** on the graph below. Identify all layers clearly.



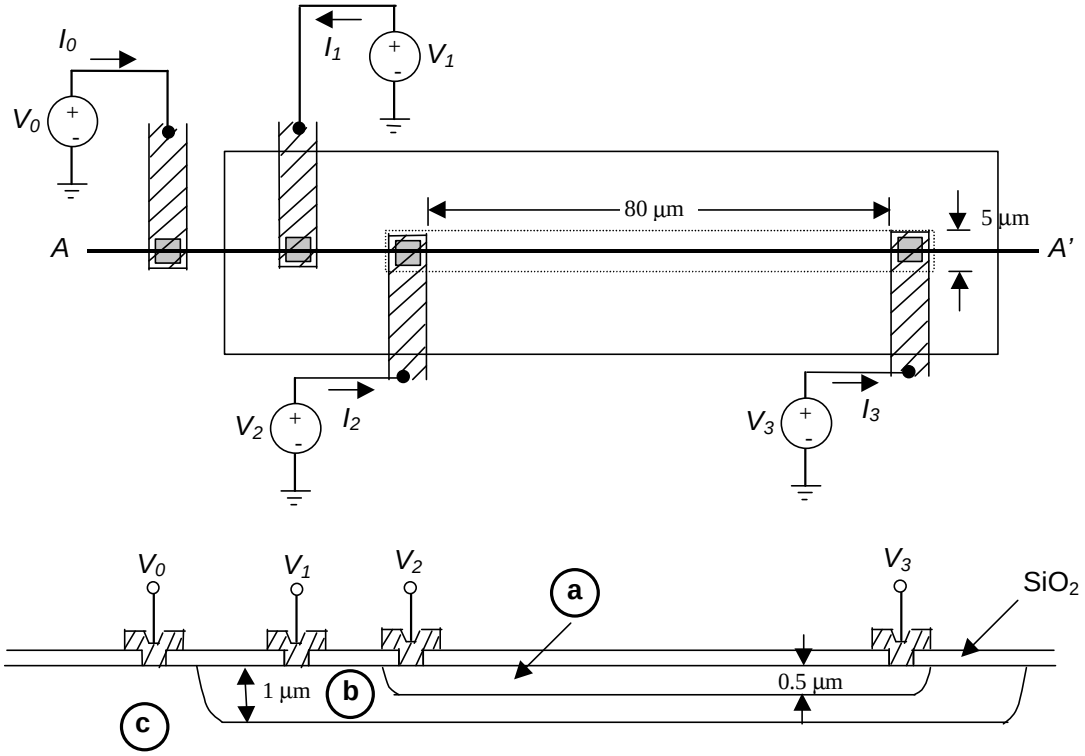
(b) [7 pts.] Sketch the cross section ***B-B'*** on the graph below. Identify all layers clearly.



(c) [3 pts.] Find the numerical value of the capacitance between terminals 1 and 2 in femtoFarads (fF). Use the layout on p. 2 to estimate the area of the capacitor. Note that the substrate is grounded, so it has no contribution to the answer to this part. Hint: terminal 1 is connected to a poly2 structure, whereas terminal 2 is connected to a poly1 structure. The capacitance is between the two polysilicon structures.

(d) [3 pts.] Find the numerical value of the capacitance between terminal 3 and the substrate. Neglect the contribution from the metal layer. Hint: you are not expected to consider capacitors in series to find the answer.

2. Integrated Circuit Resistor Structure [20 points]



Doping concentrations and thicknesses of regions **a**, **b**, and **c**:

a 3×10^{17} cm^{-3} boron, 2.5×10^{17} cm^{-3} phosphorus (0.5 μm thick)
b 10^{17} cm^{-3} boron, 2.5×10^{17} cm^{-3} phosphorus (1 μm thick)
c 10^{17} cm^{-3} boron (substrate)

Given
Electron mobility: $\mu_n = 1000$ $cm^2/(Vs)$ Hole mobility: $\mu_p = 400$ $cm^2/(Vs)$
Unit charge: $q = 1.6 \times 10^{-19}$ C

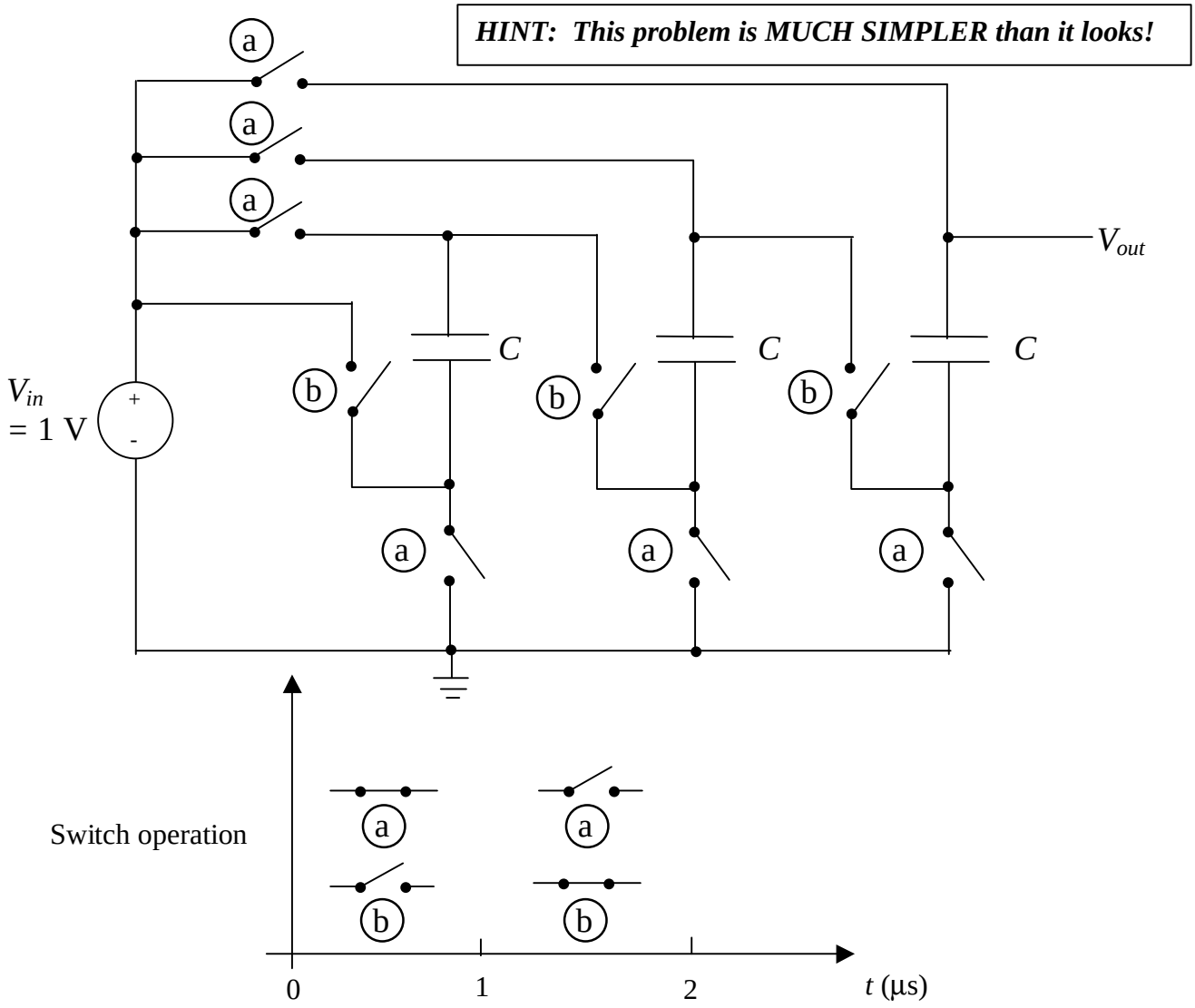
(a) [2 pts.] What is the type (n or p) and the sheet resistance of layer **a** in the IC structure whose layout and cross section is shown in the figure?

(b) [2 pts.] What is the type (n or p) and the sheet resistance of layer **b** in the IC structure whose layout and cross section is shown in the figure?

(c) [16 pts.] Fill in the table with the numerical value of the currents I_0, I_1, I_2, and I_3 in μA for the two sets of voltages. If you couldn't solve parts (a) and (b), you can assume for this part that $R_{,a} = 250\ \Omega/$ for layer a and $R_{,b} = 100\ \Omega/$. Needless to say, these are *not* the correct answers to parts (a) and (b). Hint: some of the answers are zero.

(Volts)				(MicroAmps)			
V_0	V_1	V_2	V_3	I_0	I_1	I_2	I_3
0	2	1	0.5				
3	7	0.75	3.5				

3. Switched capacitor circuit [10 points]



(a) [3 pts.] Find the charge stored on each capacitor at the time t = 0.5 μs, given that C = 50 fF and V_{in} = 1 V. Hint: draw the circuit at that time, using the switch states given above.

(b) [3 pts.] Find the charge stored on each capacitor at the time t = 1.5 μs, given that C = 50 fF and V_{in} = 1 V. The same hint from part (a) applies.

(c) [4 pts.] Find the output voltage V_{out} at the time t = 1.5 μs, given that C = 50 fF and V_{in} = 1 V. The same hint from part (a) applies.